DDR4-1.20V

SO DIMM Module

8 GB based on 8Gbit component

FBGA with Pb-Free

Revision 5.5 (Aug, 2022)
-Initial Release

260-Pin SO DIMM DDR4 SDRAM

1.0 Feature

- Power Supply: VDD=1.20V
- VPP=2.5V (NOM)
- VDDSPD=2.5V (NOM)
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- Data transfer rates: PC4-3200
- Single-rank
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- On-board I2C serial presence-detect (SPD) EEPROM
- On-die VREFDQ generation and calibration
- Selectable BC4 or BL8 on-the-fly (OTF)
- RoHS compliant & Halogen Free
- DIMM Dimension (Nominal) 30.00 mm high, 69.60 mm wide
- Fly-by topology
- Terminated control command and address bus
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
ZM4G6S8062ER	8GB	1Gx64	1Gx8 (MT40A1G8SA-062E:R)*8	FBGA	1	8GB 1Rx8 PC4-3200S

3.0 Key Timing Parameters

	DDR4-3200	Unit
CL-tRCD-tRP	22-22-22	tCK
CAS Latency	22	tCK
tCK	0.620	ns
tRCD	13.75	ns
tRP	13.75	ns
tRC	45.75	ns

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4.0 Address Configuration

Device configuration	Bank Group Address	Row Address	Column Address	Bank Address	Module Rank Address
1Gx8 (8Gb),16 Banks	4 BG[1:0]	64K A[15:0]	1K A[9:0]	4 BA[1:0]	CS0_n

5.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
Vin , Vout	Voltage on any pin relative to VSS	-0.4 ~ 1.5	V
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-0.4 ~ 1.5	V
V_{DDQ}	Voltage on VDD pin relative to Vss	-0.4 ~ 1.5	V
V_{PP}	Voltage on VPP pin relative to Vss	-0.4 ~ 3.0	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

6.0 DIMM Pin Configurations (Front side/Back side)

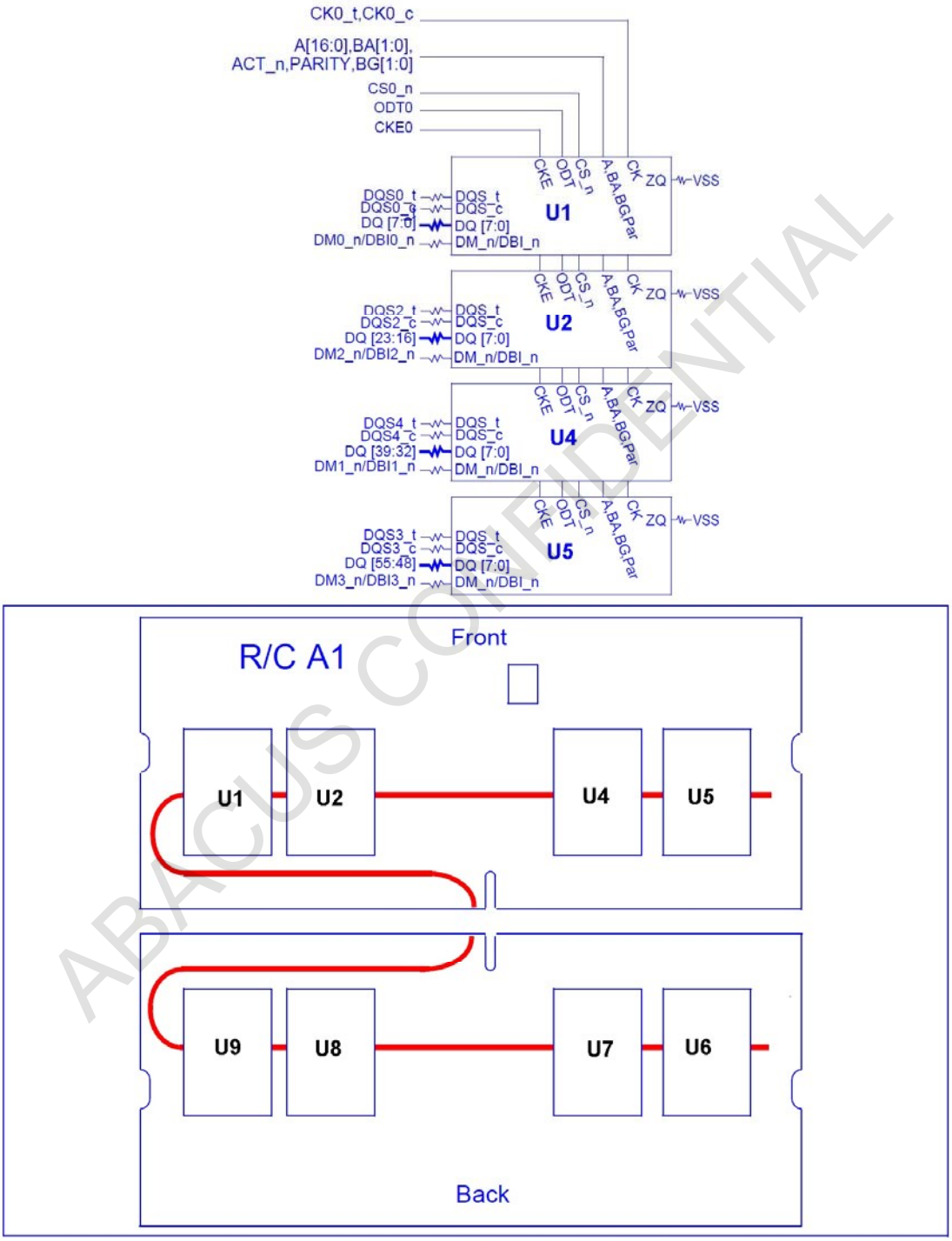
Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	65	VSS	66	DQ28
3	DQ5	4	DQ4	67	DQ29	68	VSS
5	VSS	6	VSS	69	VSS	70	DQ24
7	DQ1	8	DQ0	71	DQ25	72	VSS
9	VSS	10	VSS	73	VSS	74	DQS3_c
11	DQS0_c	12	DM0_n,DBI0_n	75	DM3_n,DBI3_n	76	DQS3_t
13	DQS0_t	14	VSS	77	VSS	78	VSS
15	VSS	16	DQ6	79	DQ30	80	DQ31
17	DQ7	18	VSS	81	VSS	82	VSS
19	VSS	20	DQ2	83	DQ26	84	DQ27
21	DQ3	22	VSS	85	VSS	86	VSS
23	VSS	24	DQ12	87	CB5,NC	88	CB4,NC
25	DQ13	26	VSS	89	VSS	90	VSS
27	VSS	28	DQ8	91	CB1,NC	92	CB0,NC
29	DQ9	30	VSS	93	VSS	94	VSS
31	VSS	32	DQS1_c	95	DQS8_c	96	DM8_n,DBI8_n
33	DM1_n,DBI1_n	34	DQS1_t	97	DQS8_c	98	VSS
35	VSS	36	VSS	99	VSS	100	CB6,NC
37	DQ15	38	DQ14	101	CB2,NC	102	VSS
39	VSS	40	VSS	103	VSS	104	CB7,NC
41	DQ10	42	DQ11	105	CB3,NC	106	VSS
43	VSS	44	VSS	107	VSS	108	RESET_n
45	DQ21	46	DQ20	109	CKE0	110	CKE1
47	VSS	48	VSS	111	VDD	112	VDD
49	DQ17	50	DQ16	113	BG1	114	ACT_n
51	VSS	52	VSS	115	BG0	116	ALERT_n
53	DQS2_c	54	DM2_n,DBI2_n	117	VDD	118	VDD
55	DQS2_t	56	VSS	119	A12	120	A11
57	VSS	58	DQ22	121	A9	122	A7
59	D123	60	VSS	123	VDD	124	VDD
61	VSS	62	DQ18	125	A8	126	A5
63	DQ19	64	VSS	127	A6	128	A4

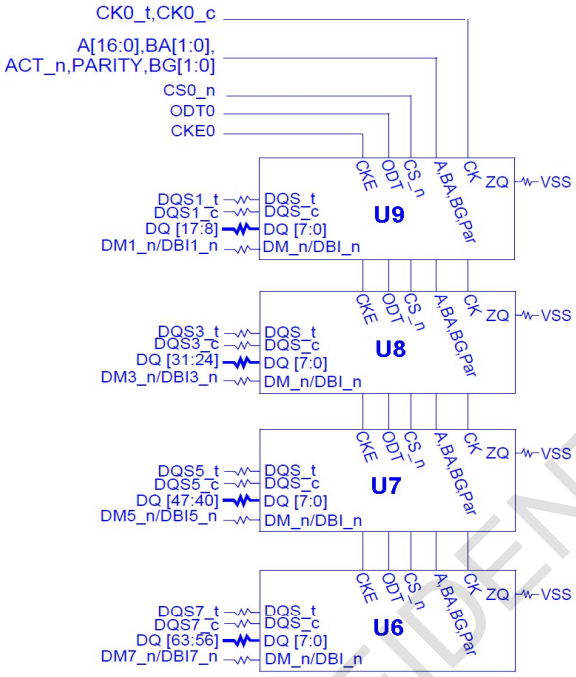
Pin	Front	Pin	Back	Pin	Front	Pin	Back
129	VDD	130	VDD	137	CK0_t	138	CK1_t
131	A3	132	A2	139	CK0_c	140	CK1_c
133	A1	134	EVENT_n	141	VDD	142	VDD
135	VDD	136	VDD	143	PARITY	144	A0
145	BA1	146	A10/AP	203	DQ46	204	DQ47
147	VDD	148	VDD	205	VSS	206	VSS
149	CS0_n	150	BA0	207	DQ42	208	DQ43
151	A14/WE_n	152	A16/RAS_n	209	VSS	210	VSS
153	VDD	154	VDD	211	DQ52	212	DQ53
155	ODT0	156	A15/CAS_n	213	VSS	214	VSS
157	CS1_n	158	A13	215	DQ49	216	DQ48
159	VDD	160	VDD	217	VSS	218	VSS
161	ODT1	162	C0,CS2_n,NC	219	DQS6_c	220	DM6_n,DBI6_n
163	VDD	164	VREFCA	221	DQS6_t	222	VSS
165	C1,CS3_n,NC	166	SA2	223	VSS	224	DQ54
167	VSS	168	VSS	225	DQ55	226	VSS
169	DQ37	170	DQ36	227	VSS	228	DQ50
171	VSS	172	VSS	229	DQ51	230	VSS
173	DQ33	174	DQ32	231	VSS	232	DQ60
175	VSS	176	VSS	233	DQ61	234	VSS
177	DQS4_c	178	DM4_n,DBI4_n	235	VSS	236	DQ57
179	DQS4_t	180	VSS	237	DQ56	238	VSS
181	VSS	182	DQ39	239	VSS	240	DQS7_c
183	DQ38	184	VSS	241	DM7_n,DBI7_m	242	DQS7_t
185	VSS	186	DQ35	243	VSS	244	VSS
187	DQ34	188	VSS	245	DQ62	246	DQ63
189	VSS	190	DQ45	247	VSS	248	VSS
191	DQ44	192	VSS	249	DQ58	250	DQ59
193	VSS	194	DQ41	251	VSS	252	VSS
195	DQ40	196	VSS	253	SCL	254	SDA
197	VSS	198	DQS5_c	255	VDDSPD	256	SA0
199	DM5_n,DBI5_n	200	DQS5_t	257	VPP	258	VTT
201	VSS	202	VSS	259	VPP	260	SA1

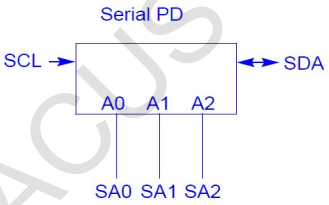
7.0 DIMM Pin Description

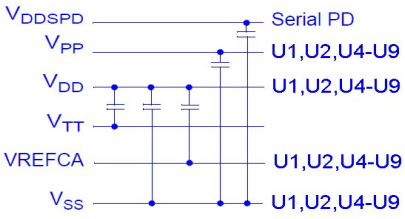
Pin Name	Function	Pin Name	Function
Ax	Address inputs	SDA	Serial Data
A10/AP	Auto precharge:	DQS_t,DQS_c, DQSU_t DQSU_c, DQSL_t, DQSL_c	Data strobe
A12/BC_n	Burst chop	ALERT_n	Alert output
ACT_n	Command input	EVENT_n	Temperature event
BAx	Bank address inputs	VDD	Module power Supply
BGx	Bank group address inputs	VPP	DRAM activating power supply
C0, C1, C2	Chip ID	VREFCA	Reference voltage for control, command, and address pins.
CKx_t CKx_c	Clock	VSS	Ground
CKEx	Clock enable	VTT	Power supply for termination of address, command, and control VDD/2
CSx_n	Chip select	VDDSPD	Power supply used to power the I2C bus for SPD.
ODTx	On-die termination	RFU	Reserved for future use
PARITY	Parity for command and address	NC	No connect
RAS_n/A16 CAS_n/A15 WE_n/A14	Command inputs	NF	No function
RESET_n	Active LOW asynchronous reset		
SAx	Serial address inputs		
SCL	Serial clock for temperature sensor/SPD EEPROM		
DQx, CBx	Data input/output and check bit input/output		
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n)	Input data mask and data bus inversion		

8.0 Functional Block Diagram: 8 GB, 1Gx64 Module (Populated as 1 rank ofx8)









Note 1: Unless otherwise noted, resistor values are 15 Ω ± 5%.
Note 2: ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.

9.0 Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V
I_{VTT}	Termination reference current from V_{TT}	–500	–	500	mA
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V
IIN	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	–2.0	–	2.0	µA
IZQ	Input leakage current; ZQ	–50.0	–	10.0	µA
IOZpd	Output leakage current; V_{OUT} = V_{DD}; DQ is High-Z	–	–	10.0	µA
IOZpu	Output leakage current; V_{OUT} = V_{SS}; DQ is High-Z; ODT is disabled with ODT input HIGH	–50.0	–	–	µA
IVREFCA	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	–2.0	–	2.0	µA

9.1 SPEED EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Typ	Max	Units
Supply voltage	VDDSPD	1.7	2.5	3.6	V
Input low voltage: logic 0; All inputs	VIL	–0.5	–	VDDSPD × 0.3	V
Input high voltage: logic 1; All inputs	VIH	VDDSPD × 0.7	–	VDDSPD + 0.5	V
Output low voltage: 3mA sink current V_{DDSPD} > 2V	VOL	–	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	ILI	–	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	ILO	–	–	±5	µA

9.2 SPEED EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	tSCL	10	1000	kHz
Clock pulse width HIGH time	tHIGH	260	–	ns
Clock pulse width LOW time	tLOW	500	–	ns
Detect clock LOW timeout	tTIMEOUT	25	35	ms
SDA rise time	tR	–	120	ns
SDA fall time	tF	–	120	ns
Data-in setup time	tSU:DAT	50	–	ns
Data-in hold time	tHD:DI	0	–	ns
Data out hold time	tHD:DAT	0	350	ns
Start condition setup time	tSU:STA	260	–	ns
Start condition hold time	tHD:STA	260	–	ns
Stop condition setup time	tSU:STO	260	–	ns
Time the bus must be free before a new transition can start	tBUF	500	–	ns
Write time	tW	–	5	ms
Warm power cycle time off	tPOFF	1	–	ms
Time from power-on to first command	tINIT	10	–	ms

12.0 SPD EEPROM Operation

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module-specific parameters
2	256–319	100h–13Fh	Reserved; all bytes coded as 00h
IDD4W	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

11. Thermal Characteristics

Symbol	Parameter/Condition	Value	Units
TC	Commercial operating case temperature	0 to 85	°C
TC	Auto precharge:	>85 to 95	°C
TOPER	Normal operating	0 to 85	°C
TOPER	Extended temperature	>85 to 95	°C
TSTG	Non-operating storage temperature	–55 to 100	°C
RHSTG	Non-operating storage relative humidity (non-	5 to 95	%
NA	Change rate of storage temperature	20	°C/hour

12.0 IDD Specifications

Specifications and Conditions – 8 GB (Die Revision R)

Parameter	Symbol	IDD	Unit
One bank ACTIVATE-PRECHARGE current	IDD0	384	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I_{PP} current	IPP0	32	mA
One bank ACTIVATE-READ-PRECHARGE current	IDD1	440	mA
Pre charge standby current	IDD2N	304	mA
Pre charge standby ODT current	IDD2NT	328	mA
Pre charge power-down current	IDD2P	240	mA
Pre charge quiet standby current	IDD2Q	272	mA
Active standby current	IDD3N	344	mA
Active standby I_{PP} current	IPP3N	24	mA
Active power-down current	IDD3P	264	mA
Burst read current	IDD4R	984	mA
Burst write current	IDD4W	848	mA
Burst refresh current (1x REF)	IDD5R	376	mA

Burst refresh I_{PP} current (1x REF)	IPP5R	40	mA
Self refresh current: Normal temperature range (0°C to +85°C)	IDD6N	256	mA
Self refresh current: Extended temperature range (0°C to +95°C)	IDD6E	416	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	IDD6R	152	mA
Auto self refresh current (25°C)	IDD6A	64	mA
Auto self refresh current (45°C)	IDD6A	152	mA
Auto self refresh current (75°C)	IDD6A	232	mA
Auto self refresh current (95°C)	IDD6A	416	mA
Auto self refresh I_{PP} current	IPP6X	40	mA
Bank interleave read current	IDD7	1240	mA
Bank interleave read I_{PP} current	IPP7	64	mA
Maximum power-down current	IDD8	192	mA

13.0 Physical Dimensions: (1Gx8 Based, 1Gx64, 1 Rank)