DDR5-1.10V

RDIMM Module

16 GB based on 16Gbit component

FBGA with Pb-Free

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Revision 1.0 (Feb, 2023)
-Initial Release

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1.0 Feature

- **DRAM VDD/VDDQ = 1.1V (-33mV / +66mV)**
- **DRAM VPP = 1.8 (–54mV / +108mV)**
- **32 Bank**
- **8 BG(Bank Group)**
- **Data transfer rates: PC5-4800**
- **BL16, BC8 OTF, BL32, BL32 OTF supported**
- **Temperature Encoding**
- **Same Bank Refresh**
- **Vref DQ / Vref CA / Vref CS Training**
- **Hard/Soft Post Package Repair**
- **Input Clock Frequency Change**
- **Maximum Power Saving Mode (MPSM)**
- **Multi-Purpose Command (MPC)**
- **Per DRAM Addressability (PDA)**
- **Read Training Mode**
- **CA Training Mode**
- **CS Training Mode**
- **Per Pin VREFDQ Training**
- **Write Leveling Training Mode**
- **Connectivity Test (CT)**
- **ZQ Calibration**
- **DFE (Decision Feedback Equalization) for DQ**
- **DQS Interval Oscillator**
- **1N / 2N Mode support for Commands**
- **On-Die ECC**
- **ECC Transparency and Error Scrub**
- **CRC (Cyclic Redundancy Check)**
- **Loopback for multiple purposes - monitor data, BER (Bit Error Rate) analysis, etc.**
- **Package Output Driver Test Mode**
- **Training Modes:**
    - VrefDQ / VrefCA / VrefCS Training
    - Read Training Mode
    - CA Training Mode
    - CS Training Mode
    - Per Pin VREFDQ Training
    - Write Leveling Training Mode
    - Duty Cycle Adjuster (DCA) for Read - Global
    - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)
- **sPPR Do / Undo / Lock**
- **MBIST / mPPR**

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- 0.5*CK Write Levling Internal Cycle Alignment
- Partial Array Self Refresh (PASR)
- NOT supported Adaptive Refresh Management (ARFM)
- NOT supported Refresh Interval Rate Indicator
- NOT required RFM
- This product is in Compliance with the RoHS directive
- DIMM Dimension (Nominal) 31.25 mm high, 133.35 mm wide
- Based on JEDEC standard
- RoHS compliant & Halogen Free
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
ZHMCG78AEBR168Y1	16 GB	2Gx80	2Gx8 (H5CG48AEBDX018)*10	FBGA	1	16GB 1Rx8 PC5-4800R

3.0 Key Timing Parameters

	DDR5-4800	Unit
CL-tRCD-tRP	40-39-39	tCK
tAA	16.00	ns
tCK	0.416	ns
tRCD	16.00	ns
tRP	16.00	ns
tRAS	32.00	ns
tRC	48.00	ns

4..0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V
VIN, VOUT	Voltage on any pin relative to Vss	-0.3 ~ 1.4	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 Address Configuration

Organization	Bank Group Address	Row Address	Column Address	Bank Address	Page Size
2Gx80 (16 Gb) base	BG0~BG2	R0-R15	C0-C9	BA0-BA1	1 KB

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6.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VIN_BULK	49	DQ29_A	97	CB0_B	145	VIN_BULK	193	VSS	241	VSS
2	RFU	50	VSS	98	VSS	146	VIN_BULK	194	DQ31_A	242	CB2_B
3	RFU	51	CB0_A	99	CB1_B	147	PWR_GOOD	195	VSS	243	VSS
4	HSCL	52	VSS	100	VSS	148	HSA	196	CB2_A	244	CB3_B
5	HSDA	53	CB1_A	101	DQ0_B	149	RFU	197	VSS	245	VSS
6	VSS	54	VSS	102	VSS	150	VSS	198	CB3_A	246	DQ2_B
7	RFU	55	DQS4_A_c	103	DQ1_B	151	PWR_EN	199	VSS	247	VSS
8	VSS	56	DQS4_A_t	104	VSS	152	RFU	200	ALERT_n	248	DQ3_B
9	DQ0_A	57	VSS	105	DQS0_B_c	153	VSS	201	VSS	249	VSS
10	VSS	58	CS0_A_n	106	DQS0_B_t	154	DQ2_A	202	CS1_A_n	250	DM0_B_n
11	DQ1_A	59	VSS	107	VSS	155	VSS	203	VSS	251	VSS
12	VSS	60	CA0_A	108	DQ4_B	156	DQ3_A	204	CA1_A	252	DQ6_B
13	DQS0_A_c	61	CA2_A	109	VSS	157	VSS	205	CA3_A	253	VSS
14	DQS0_A_t	62	VSS	110	DQ5_B	158	DM0_A_n	206	VSS	254	DQ7_B
Pin	**Front**	**Pin**	**Front**	**Pin**	**Front**	**Pin**	**Back**	**Pin**	**Back**	**Pin**	**Back**
15	VSS	63	CA4_A	111	VSS	159	VSS	207	CA5_A	255	VSS
16	DQ4_A	64	CA6_A	112	DQ8_B	160	DQ6_A	208	CA7_A	256	DQ10_B
17	VSS	65	VSS	113	VSS	161	VSS	209	VSS	257	VSS
18	DQ5_A	66	CA8_A	114	DQ9_B	162	DQ7_A	210	CA9_A	258	DQ11_B
19	VSS	67	CA10_A	115	VSS	163	VSS	211	CA11_A	259	VSS
20	DQ8_A	68	VSS	116	DM1_B_n	164	DQ10_A	212	VSS	260	DQS1_B_c
21	VSS	69	CA12_A	117	VSS	165	VSS	213	RFU	261	DQS1_B_t
22	DQ9_A	70	RFU	118	DQ12_B	166	DQ11_A	214	RFU	262	VSS
23	VSS	71	VSS	119	VSS	167	VSS	215	VSS	263	DQ14_B
24	DM1_A_n	72	CK0_A_t	120	DQ13_B	168	DQS1_A_c	216	CK1_A_t	264	VSS
25	VSS	73	CK0_A_c	121	VSS	169	DQS1_A_t	217	CK1_A_c	265	DQ15_B
26	DQ12_A	74	VSS	122	DQ16_B	170	VSS	218	VSS	266	VSS
27	VSS	75	RFU	123	VSS	171	DQ14_A	219	RFU	267	DQ18_B
28	DQ13_A	76	RFU	124	DQ17_B	172	VSS	220	RFU	268	VSS
29	VSS	77	VSS	125	VSS	173	DQ15_A	221	VSS	269	DQ19_B
30	DQ16_A	78	CK0_B_t	126	DQS2_B_c	174	VSS	222	CK1_B_t	270	VSS
31	VSS	79	CK0_B_c	127	DQS2_B_t	175	DQ18_A	223	CK1_B_c	271	DM2_B_n
32	DQ17_A	80	VSS	128	VSS	176	VSS	224	VSS	272	VSS
33	VSS	81	RFU	129	DQ20_B	177	DQ19_A	225	RFU	273	DQ22_B
34	DQS2_A_c	82	CA12_B	130	VSS	178	VSS	226	RFU	274	VSS
35	DQS2_A_t	83	VSS	131	DQ21_B	179	DM2_A_n	227	VSS	275	DQ23_B
36	VSS	84	CA10_B	132	VSS	180	VSS	228	CA11_B	276	VSS
37	DQ20_A	85	CA8_B	133	DQ24_B	181	DQ22_A	229	CA9_B	277	DQ26_B
38	VSS	86	VSS	134	VSS	182	VSS	230	VSS	278	VSS
39	DQ21_A	87	CA6_B	135	DQ25_B	183	DQ23_A	231	CA7_B	279	DQ27_B
40	VSS	88	CA4_B	136	VSS	184	VSS	232	CA5_B	280	VSS
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back

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41	DQ24_A	89	VSS	137	DM3_B_n	185	DQ26_A	233	VSS	281	DQS3_B_c
42	VSS	90	CA2_B	138	VSS	186	VSS	234	CA3_B	282	DQS3_B_t
43	DQ25_A	91	CA0_B	139	DQ28_B	187	DQ27_A	235	CA1_B	283	VSS
44	VSS	92	VSS	140	VSS	188	VSS	236	VSS	284	DQ30_B
45	DM3_A_n	93	CS0_B_n	141	DQ29_B	189	DQS3_A_c	237	CS1_B_n	285	VSS
46	VSS	94	VSS	142	VSS	190	DQS3_A_t	238	VSS	286	DQ31_B
47	DQ28_A	95	RESET_n	143	RFU	191	VSS	239	DQS4_B_c	287	VSS
48	VSS	96	VSS	144	RFU	192	DQ30_A	240	DQS4_B_t	288	RFU

7.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
CA[6:0]_A CA[6:0]_B	SDRAM Address and Command Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A CS[1:0]_B	SDRAM Chip Select	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A &
PAR_A	SDRAM Parity input	DQS[9:0]_A_t	SDRAM Data Strobes
CK_t	SDRAM Clocks (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	SDRAM Data Strobes (negative line of differential pair)
CK_c	SDRAM Clocks (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	SDRAM alert for CRC error	TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state	VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port	VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data	RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address	LBDQS	Power supply return (ground)
LBDQ	Loopback Data output:		

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8.0 Input/output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A CA[6:0]_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multicycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the opcode during Mode Register Set commands.
CS[1:0]_A CS[1:0]_B	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command codes. CS_n is also used to enter and exit the parts from power down mode and self-refresh mode. While not in self-refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self-refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR_A PAR_B	Input	Command and Address Parity Input: DDR5 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CSx_x_n LOW
ALERT_n	Output	Alert: If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Input/ Output	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
HSCL	Input	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	Input/ Output	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	Input	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation

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Symbol	Type	Function
DQ[31:0]_A DQ[31:0]_B	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/ Output	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating
DQS[9:0]_A_t DQS[9:0]_B_t	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
DQS[9:0]_A_c DQS[9:0]_B_c		
TDQS[9:5]_A_t TDQS[9:5]_B_t	Input/ Output	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.
TDQS[9:5]_A_c TDQS[9:5]_B_c		
DLBDQ	Output	Loopback Data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled the pin is either terminated or Hi-Z based on MR36: OP[2:0].
DLBDQS	Output	Loopback Data Strobe output: This is a single ended strobe with the rising edged aligned with Loopback Data edge, falling edge aligned with Data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36: OP[2:0].
RFU		Reserved for Future Use: No on DIMM electrical connection is present.
VIN BULK	Supply	External power supply: 12V, 4.25V (min), 15V (max)
VIN_MGMT	Supply	External power supply: 3.3V, 3.0V (min), 3.6V (max)
VSS	Supply	Ground

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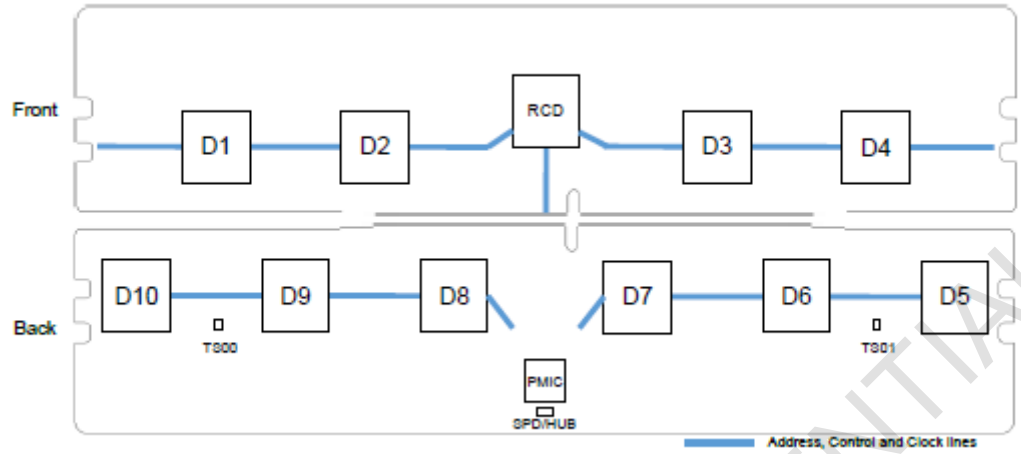
9.0 Functional Block Diagram: 16 GB, 2Gx80 Module (Populated as 1 Rank ofx8)



10.0 DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz	
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm

11.0 Standard Speed Bins

Speed Bin CL-nRCD-nRP Parameter	Symbol	DDR5-4800B 40-39-39 min	max	Unit
Internal read command to first data	tAA	16.000	22.222	ns
ACT to internal read or write delay time	tRCD	16.000	-	ns
Row Precharge Time	tRP	16.000	-	ns
ACT to PRE command period	tRAS	32.00	5 x	ns

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						tREFI1	
ACT to ACT or REF command period				tRC	48.000	-	ns
CAS Write Latency				CWL	CWL=CL-2		ncK
Speed Bin	tAAmin| (ns)	tRCDmin tRPmin (ns)	Read CL	Supported Frequency Down Bins			
	20.952	-	22	tCK(AVG)	0.952	1.010	ns
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns
3200BN 3200B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns
3600BN 3600B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns
4000BN 4000B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns
4400BN 4400B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED		ns

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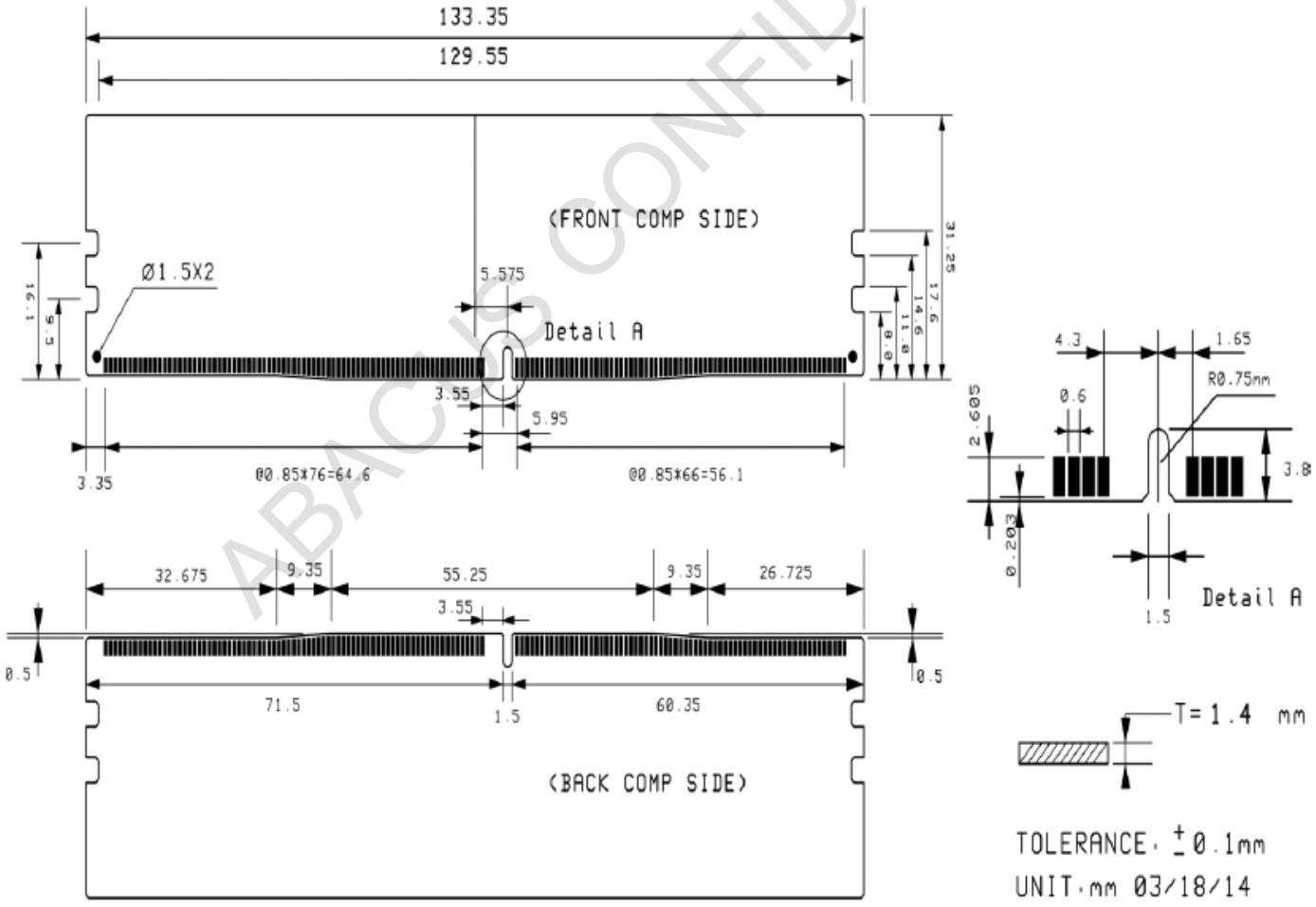
Supported CL	22,26,28,30,32,36,38,40,42,	nCK

12.0 Environmental Parameters

Symbol	Parameter	Rating	Units
T_{OPR}	Operating temperature (ambient)	0 to +95	^{o}C
H_{OPR}	Operating humidity (relative)	10 to 90	%
T_{STG}	Storage temperature	-55 to +100	^{o}C
H_{STG}	Storage humidity (without condensation)	5 to 95	%
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal

13.0 Physical Dimensions: (2Gx8 Based, 2Gx80, 1 Ranks)



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