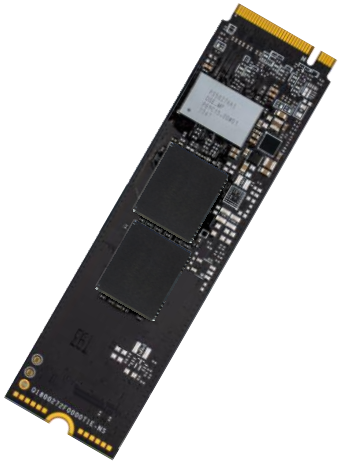
ABACUS PERIPHERALS PVT LTD

ABSNE27-E27T PCIe M.2 2280 KIOXIA BiCS6 Specification (ABSNE271024KP/ABSNE27512KP) (Series - ABSNE27)

Version 1.3



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Document Number: Abacus/SSD/DS/09

REVISION HISTORY

Revision	Draft Date	History
1.0	2024/02/01	First release
1.1	2024/05/15	Add series number
1.2	2024/05/15	Remove 2048GB,256GB
1.3	2024/05/20	Series Correction

PRODUCT OVERVIEW

- Capacities
  - 512, 1024GB
- Form Factor
  - M.2 2280-S2-M
- PCIe Interface
  - PCIe Gen 4 x 4
- Compliance
  - NVMe 1.4
  - PCI Express Base 4.0
- Flash Interface
  - Transfer rate up to 2400MT/s
  - Up to 2pcs of BGA154 flash
- Performance[1]
  - Read: up to 7400 MB/s
  - Write: up to 6400 MB/s
- Reliability
  - Mean Time Between Failure (MTBF): 1,500,000 hours
  - Uncorrectable Bit Error Rate (UBER): < 1 sector per 1016 bits read
- Temperature Range[3]
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- Advanced Flash Management
  - Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
  - Firmware Update
- Power Management
  - PS0/PS1/PS2/PS3/PS4
  - Support APST
  - Support ASPM
  - Support L1.2
- Power Consumption[2]
  - L1.2 < 5mW
- RoHS-Compliant
- Features Support List:
  - All SRAM ECC protection
  - Thermal throttling
  - LDPC + RAID ECC
  - SmartRefresh™
  - Drive log
  - Support HMB (Host Memory Buffer)
  - Support of TCG Pyrite

NOTES:
1. Refer to Chapter 2 for more details
2. Refer to Chapter 4, Section for more details.
3. The operation temperature means the case temperature, in which can be decided via the S.M.A.R.T.

PERFORMANCE

KIOXIA BiCS6 1024Gb TLC (2400MBps)

Capacity	Flash Structure	Sequential (Estimation)		Random (Estimation)		ATTO	
		Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)	Read (MB/s)	Write (MB/s)
512GB	256GB x 2, 4CE	7200	4300	530K	750K	7000	5000
1024GB	512GB x 2, 8CE	7400	6100	1000K	850K	7000	5000

NOTES:

1. Performance is measured based on the following conditions:
   (a) Sequential: CrystalDiskMark 8.0, 1GB range, 5 test count, Q8T1
   (b) Random: IOMeter, 1GB range, 4K data size, QD=32T16
   (c) ATTO, transfer Size 64MB
   (d) CPU: AMD Ryzen 7 5800X 8-Core Processor
   (e) OS Version: Win10 (64bit), version 1809
   (f) Platform : AMD X570
   (g) Performance is measured with fresh-out-of-box state SSD storage device.

POWER CONSUMPTION

KIOXIA BiCS6 1024Gb TLC (2400MBps)

Capacity	Flash Configuration	Power Consumption[1]			
		Read (mW)	Write (mW)	PS3 (mW)	PS4 (mW)
512GB	BGA154, KIC BiCS6, DDP*2	5150	4300	50	5
1024GB	BGA154, KIC BiCS6, QDP*2	5600	5400	50	5

NOTES:

1. Power consumption is measured during the sequential read and write operations performed by IOMeter under ambient temperature @25°C.

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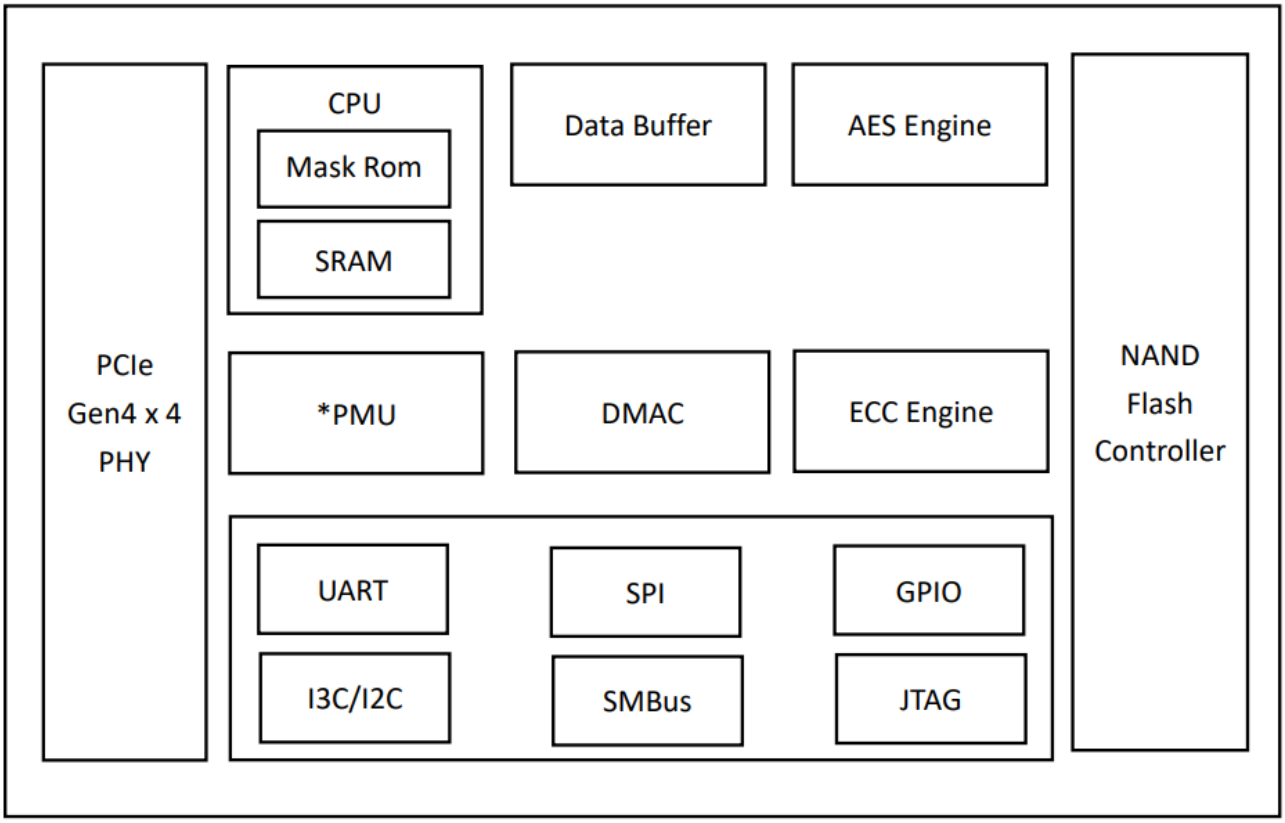
1. INTRODUCTION

1.1. General Description

PS5027-E27T M.2 2280 with no external DDR solution delivers all the advantages of flash disk technology with PCIe Gen4 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. PS5027-E27T M.2 2280 offers a wide range of capacities up to 1024GB and its performance can reach up to 7400 MB/s[1] and 6400 MB/s[1] based on KIC BiCS6 1024Gb TLC NAND flash. NOTES:

1. Achieved by 1024GB SSD at FOB (fresh-out-of-box) state on CrystalDiskMark v8.0.

1.2. Controller Block Diagram



*PMU = Power Management Unit

Figure 1-1 PS5027-E27T Controller Block Diagram

1.3. Product Block Diagram

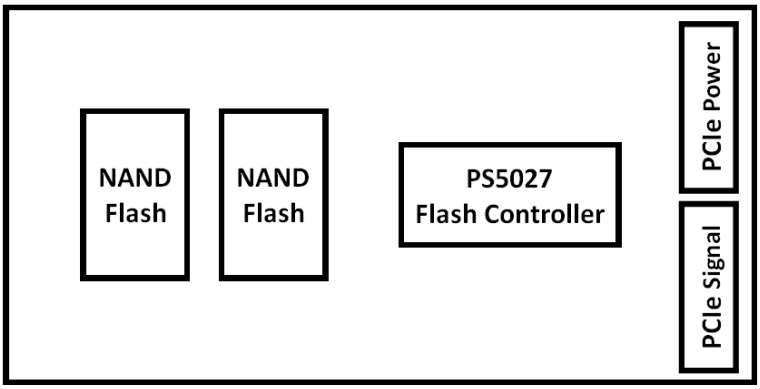


Figure 1-2 PS5027-E27T M.2 2280 Product Block Diagram

1.4. Flash Management

1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS5027-E27T PCIe SSD applies the LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.4.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Abacus provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.4.3. Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named

"Later Bad Blocks". Abacus implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

1.4.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

1.4.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

1.4.6. Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.4.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgradable when new features are added, compatibility issues are fixed, or read/write performance gets improved.

1.4.8. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. PS5027-E27T is designed with an on-die thermal sensor and with its accuracy; firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

1.5. Advanced Device Security Features

1.5.1. Secure Erase

Secure Erase is a standard NVMe format command and will write all "0x00" to fully wipe all the data on hard drives and SSDs. When this command is issued, SSD controller will erase its storage blocks and return to its factory default settings.

1.5.2. Crypto Erase

Crypto Erase is a feature that erases all data of an OPAL-activated SSD or a "SED" (Security-Enabled Disk) drive by resetting the cryptographic key of the disk. Since the key is modified, the previously encrypted data will become useless, achieving the purpose of data security.

1.5.3. Physical Presence SID (PSID)

Physical Presence SID (PSID) is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

1.6. SSD Lifetime Management

1.6.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

$$TBW = [(NAND\ Endurance) \times (SSD\ Capacity)] / [WAF]$$

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A

better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 219 workload.

1.6.2. Media Wear Indicator

Actual life indicator reported by SMART Attribute byte index [5], Percentage Used, recommends User to replace drive when reaching to 100%.

1.6.3. Read Only Mode (End of Life)

When drive is aged by cumulated program/erase cycles, media worn-out may cause increasing numbers of later bad block. When the number of usable good blocks falls outside a defined usable range, the drive will notify Host through AER event and Critical Warning to enter Read Only Mode to prevent further data corruption. User should start to replace the drive with another one immediately.

1.7. Adaptive Approach to Performance Tuning

1.7.1. Throughput

Based on the available space of the disk, PS5027-E27T will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, PS5027-E27T will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

1.7.2. SLC Caching

PS5027-E27T's firmware design currently adopts dynamic caching to deliver better performance for better endurance and consumer user experience.

2. PRODUCT SPECIFICATIONS

- Capacity
  - 512GB, 1024GB
  - Support 32-bit addressing mode
- Electrical/Physical Interface
  - PCIe Interface
  - Compliant with NVMe 1.4
  - PCIe Express Base Version 4.0
  - PCIe Gen 4 x 4 lane & backward compatible to PCIe Gen 3, PCIe Gen 2 and Gen 1
  - Support up to QD 128 with queue depth of up to 64K
  - Support power management
- Supported NAND Flash
  - Support up to 16 Flash Chip Enables (CE) within a single design
  - Support up to 2pcs of BGA154 flash
  - Support 8-bit I/O NAND Flash
  - Support Toggle5.0 interface
- ECC Scheme
  - PS5027-E27T PCIe SSD applies LDPC + RAID ECC algorithm.
- Sector Size Support
  - 512B
  - 4KB
- UART/ GPIO
- Support SMART and TRIM commands
- LBA Range
  - IDEMA standard

■ TBW (Terabytes Written)

Table 2-1 TBW of PS5027-E27T+KIOXIA BiCS6

Capacity	TBW
512GB	>300 TB
1024GB	>600 TB

■ Performance

KIOXIA BiCS6 1024Gb TLC (2400MBps)

Capacity	Flash Structure	Sequential		Random	
		Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
512GB	256GB x 2, 4CE	7200	4300	530K	750K
1024GB	512GB x 2, 8CE	7400	6100	1000K	850K

NOTES:

1. Performance is measured based on the following conditions:
   (a) Sequential: CrystalDiskMark 8.0, 1GB range, 5 test count, Q8T1
   (b) Random: IOMeter, 1GB range, 4K data size, QD=32T16
   (c) CPU: AMD Ryzen 7 5800X 8-Core Processor
   (d) OS Version: Win10 (64bit), version 1809
   (e) Platform : AMD X570
   (f) Performance is measured with fresh-out-of-box state SSD storage device.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

Table 3-1 High Temperature

	Temperature	Humidity
Operation	70°C	0% RH
Storage	85°C	0% RH

Table 3-2 Low Temperature

	Temperature	Humidity
Operation	0°C	0% RH
Storage	-40°C	0% RH

Table 3-3 High Humidity

	Temperature	Humidity
Operation	40°C	90% RH
Storage	40°C	93% RH

Table 3-4 Temperature Cycling

	Temperature
Operation	0°C
	70°C[1]
Storage	-40°C
	85°C

Notes:

1. The operation temperature is measured by the case temperature, in which can be decided via the S.M.A.R.T. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

3.1.2. Shock

Table 3-5 Shock

	Acceleration Force
Non-operational	1500G

3.1.3. Vibration

Table 3-6 Vibration

	Condition	
	Frequency/Displacement	Frequency/Acceleration
Non-operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G

3.1.4. Drop

Table 3-7 Drop

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

3.1.5. Bending

Table 3-8 Bending

	Force	Action
Non-operational	≥ 20N	Hold 1min/5times

3.1.6. Durability

Table 3-9 Durability

	Condition
operational	1000 mating cycles

3.1.7. Electrostatic Discharge (ESD)

Table 3-10 ESD

Specification	+/- 4KV
EN 55024, CISPR 24 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.8. EMI Compliance

Table 3-11 EMI

Specification
EN 55032, CISPR 32(CE) AS/NZS CISPR 32(CE) ANSI C63.4 (FCC) VCCI-CISPR 32 (VCCI) CNS 13438 (BSMI)

3.2. MTBF

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on Telcordia methodology. Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

3.3. Certification & Compliance

Table 3-12 Certification & Compliance

Specification
RoHS
WHQL
PCI Express Base 4.0
UNH-IOL NVM Express Logo

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage

Parameter	Rating
Operating Voltage	Min = 3.14V Max = 3.47 V
Rise Time (Max/Min)	100 ms / 0.1 ms
Fall Time (Max/Min)	5 s / 1 ms
Min. Off Time[1]	5 s

NOTE:

1. Minimum time between power removed from SSD (Vcc < 100 mV) and power re-applied to the drive.

4.2. Power Consumption

Table 4-2 Power Consumption with KIOXIA BiCS6 1024Gb (2400) TLC in mW

Capacity	Flash Configuration	CE#	Read		Write	
			Max.	Avg.	Max.	Avg.
512GB	BGA154, KIC BiCS6 1024Gb, DDP*2	4	TBD	TBD	TBD	TBD
1024GB	BGA154, KIC BiCS6 1024Gb, QDP*2	8	TBD	TBD	TBD	TBD

NOTES:

1. Power consumption is measured with the condition under ambient temperature @25°C.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. The measured power voltage is 3.3V.

Table 4-3 Power State Power Consumption with KIOXIA BiCS6 1024Gb (2400) TLC in mW

Capacity	Flash Configuration	CE#	Active			PS3	PS4
			PS0	PS1	PS2		
512GB	BGA154, KIC BiCS6 1024Gb, DDP*2	4	5150	3000	1700	50	5
1024GB	BGA154, KIC BiCS6 1024Gb, QDP*2	8	5600	3000	1800	50	5

NOTES:

4. Power consumption is measured with the condition under ambient temperature @25°C.
5. The average value of power consumption is achieved based on 100% conversion efficiency.
6. The measured power voltage is 3.3V.
7. The temperature of a storage device in PS1 should remain constant or should slightly decrease for all workloads so the actual power in PS1 should be lower than PS0.
8. The temperature of a storage device in PS2 should decrease sharply for all workloads so the actual power in PS2 should be lower than PS1.
9. PS3 & PS4 is specific in L1.2

Table 4-4 Mobile Mark 2023 Average Power Consumption with KIOXIA BiCS6 1024Gb (2400) TLC in mW

Capacity	Flash Structure	CE#	Primary
512GB	256GB x 2 BiCS6	4	TBD
1024GB	512GB x 2 BiCS6	8	TBD

NOTES:

1. Power consumption is measured with the condition under ambient temperature @25°C.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. The measured power voltage is 3.3V.

5. INTERFACE

5.1. Pin Assignment and Descriptions

Table 5-1 defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.0 of the PCI-SIG.

Table 5-1 Pin Assignment and Description of PS5027-E27T M.2 2280

Pin No.	PCIe Pin	Description
1	GND	Return current path.
2	3.3V	PWR_1 source
3	GND	Return current path.
4	3.3V	PWR_1 source
5	PETn3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
6	PWRDIS (I)(0/1.8/3.3V)	Active high with weak pull-down on Adapters. Power Disable notifies the Adapter to disable the power on the Adapter.
7	PETp3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
8	PLN# (I)(0/1.8/3.3V)	Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.
9	GND	Return current path.
10	LED_1# (O)(OD)	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.
11	PERn3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
12	3.3V	PWR_1 source
13	PERp3	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
14	3.3V	PWR_1 source
15	GND	Return current path.
16	3.3V	PWR_1 source
17	PETn2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
18	3.3V	PWR_1 source
19	PETp2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
20	NC	No connect
21	GND	Return current path.
22	VIO 1.8V	I/O source (low current)
23	PERn2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
24	NC	No connect

Pin No.	PCIe Pin	Description
25	PERp2	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
26	NC	No connect
27	GND	Return current path.
28	NC	No connect
29	PETn1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
30	PLA_S3# (O)(0/1.8/3.3V)	Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.
31	PETp1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
32	GND	Return current path.
33	GND	Return current path.
34	NC	No connect
35	PERn1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
36	NC	No connect
37	PERp1	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
38	GND	Return current path.
39	GND	Return current path.
40	SMB_CLK (I/O)(0/1.8V)	SMBus clock. Open Drain with pull up on Platform
41	PETn0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
42	SMB_DATA (I/O)(0/1.8V)	SMBus data. Open Drain with pull up on Platform
43	PETp0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
44	ALERT#(O) (0/1.8V)	Alert notification to initiator. Open Drain with pull up on Platform. Active Low
45	GND	Return current path.
46	NC	No connect
47	PERn0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
48	NC	No connect
49	PERp0	PCIe TX/RX Differential signals defined by the PCI Express Base Specification.
50	PERST# (I)(0/1.8V/3.3V)	PCIe Reset is a functional reset to the card as defined by the PCI Express BaseSpecification.
51	GND	Return current path.
52	CLKREQ#(I/O)(0/1.8V/3.3V)	PCIe Clock Request is a reference clock request signal as defined by the PCI Express Base Specification, also used by L1 PM Substates. Open Drain with pull up on Platform. Active Low.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Base Specification.
54	NC	No connect
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Base Specification.

Pin No.	PCIe Pin	Description
56	Reserved for MFG_DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in Platform Socket.
57	GND	Return current path.
58	Reserved for MFG_CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in Platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	NC	No connect
68	NC	No connect
69	PEDET = NC (PCIe)	Host interface Indication; to be grounded for SATA. No Connect for PCIe.
70	3.3V	PWR_1 source
71	GND	Return current path.
72	3.3V	PWR_1 source
73	VIO_CFG (O)	Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter. VIO_CFG of SSD device is default supports 3.3V on the sideband IO signals.
74	3.3V	PWR_1 source
75	GND	Return current path.

6. SUPPORTED COMMANDS

6.1. NVMe/ATA Command List

The following ATA command list table is followed by ATA8-ACS4 SPEC.

Table 6-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test

Table 6-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Table 6-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management
0Ch	Verify

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-4 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x6
75:73	M	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x06
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x10400
87:84	M	RTD3 Resume Latency (RTD3R)	0x0007A120
91:88	M	RTD3 Entry Latency (RTD3E)	0x4C4B40
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000200
99:96	M	Controller Attributes (CTRATT)	0x2
101:100	O	Read Recovery Levels Supported (RRLS)	0x0
110:102	-	Reserved	0x00
111	M	Controller Type (CNTRLTYPE)	0x1
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
129:128	O	Command Retry Delay Time 1 (CRDT1)	0x0
131:130	O	Command Retry Delay Time 2 (CRDT2)	0x0
133:132	O	Command Retry Delay Time 3 (CRDT3)	0x0
239:134	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
257:256	M	Optional Admin Command Support (OACS)	0x17
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x07
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x1E
262	M	Error Log Page Entries (ELPE)	0xFE
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x164
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x166
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0032
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x4000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x4000
295:280	O	Total NVM Capacity (TNVMCAP)	0
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000

Bytes	O/M	Description	Default Value
317:316	O	Extended Device Self-test Time (EDSTT)	0x000A
318	O	Device Self-test Options (DSTO)	0x01
319	M	Firmware Update Granularity (FWUG)	0x4
321:320	M	Keep Alive Support (KAS)	0x00
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x1
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x164
331:328	O	Sanitize Capabilities (SANICAP)	0xA0000002
335:332		Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)	0x400
337:336		Host Memory Maximum Descriptors Entries (HMMAXD)	0x10
339:338		NVM Set Identifier Maximum (NSETIDMAX)	0x0
341:340		Endurance Group Identifier Maximum (ENDGIDMAX)	0x0
342		ANA Transition Time (ANATT)	0x0
343		Asymmetric Namespace Access Capabilities (ANACAP)	0x0
347:344		ANA Group Identifier Maximum (ANAGRPMAX)	0x0
351:348		Number of ANA Group Identifiers (NANAGRPID)	0x0
355:352		Persistent Event Log Size (PELS)	0x60
511:356	-	Reserved	0
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x100
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0xDF
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x07
527:526	M	Atomic Write Unit Normal (AWUN)	0xFF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x0000
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
543:540	O	Maximum Number of Allowed Namespaces (MNAN)	0x00
767:544	M	Reserved	0x00
IO Command Set Attributes			
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	non-zero
1791:1024		Reserved	0x00
2047:1792	M	Refer to the NVMe over Fabrics specification.	0
2079:2048	M	Power State 0 Descriptor	Bit[15:0]: 0x23A
2111:2080	O	Power State 1 Descriptor	Bit[124:120]: 0x1 Bit[116:112]: 0x1 Bit[108:104]: 0x1 Bit[100:96]: 0x1 Bit[15:0]: 0x12C

Bytes	O/M	Description	Default Value
2143:2112	O	Power State 2 Descriptor	Bit[124:120]: 0x2 Bit[116:112]: 0x2 Bit[108:104]: 0x2 Bit[100:96]: 0x2 Bit[15:0]: 0xB4
2175:2144	O	Power State 3 Descriptor	Bit[124:120]: 0x3 Bit[116:112]: 0x3 Bit[108:104]: 0x3 Bit[100:96]: 0x3 Bit[95:64]: 0x9C4 Bit[63:32]: 0x1388 Bit[25]: 1 Bit[24]: 1 Bit[15:0]: 0x1F4
2207:2176	O	Power State 4 Descriptor	Bit[124:120]: 0x4 Bit[116:112]: 0x4 Bit[108:104]: 0x4 Bit[100:96]: 0x4 Bit[95:64]: 0x9C40 Bit[63:32]: 0x1F40 Bit[25]: 1 Bit[24]: 1 Bit[15:0]: 0x32
…	-	(N/A)	0
3071:3040	O	Power State 31 Descriptor	0
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Abacus Reserved

6.3. SMART Attributes

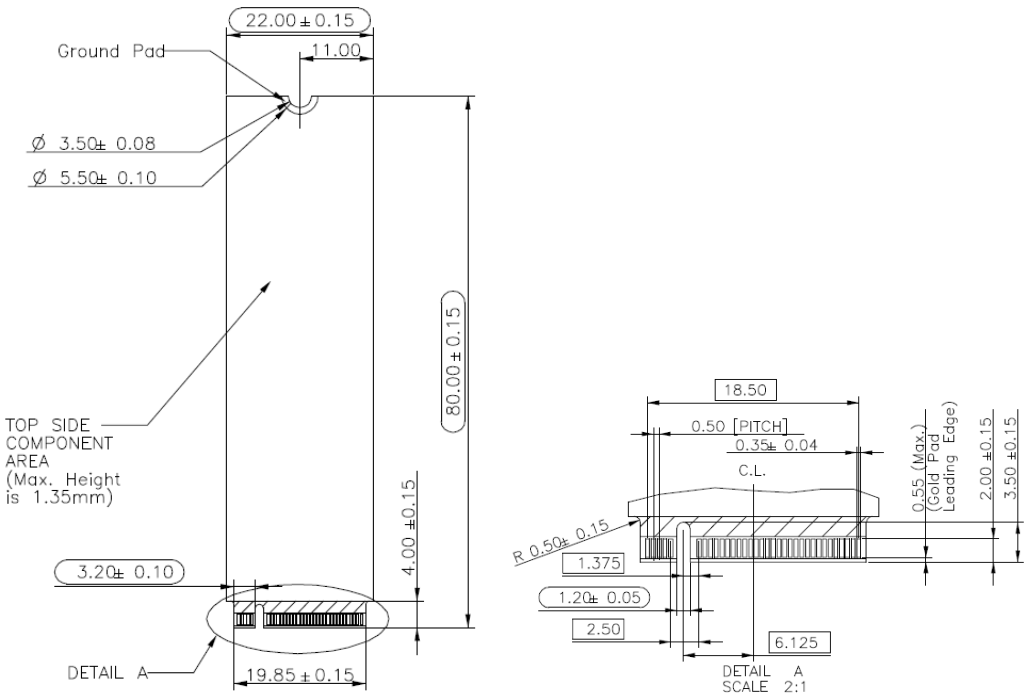
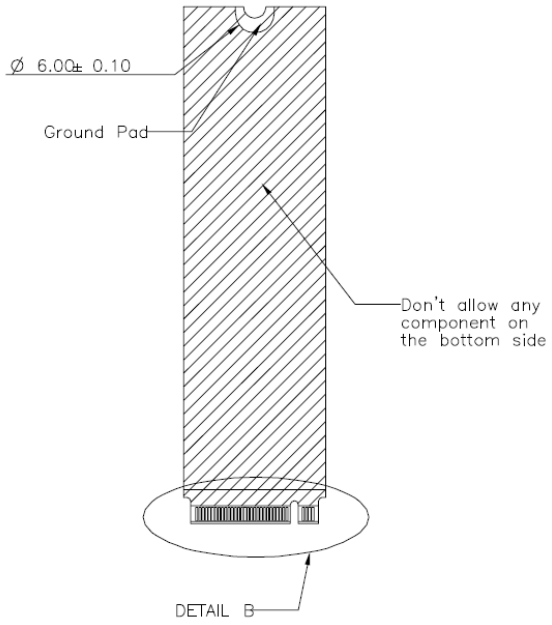
Table 6-5 SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1
[215:202]	14	Reserved
[219:216]	4	Thermal Management Temperature 1 Transition Count
[223:220]	4	Thermal Management Temperature 2 Transition Count
[227:224]	4	Total Time For Thermal Management Temperature 1
[231:228]	4	Total Time For Thermal Management Temperature 2
[511:232]	280	Reserved

7. PHYSICAL DIMENSION

Form factor: M.2 2280 S2

Dimensions: 80.00mm (L) x 22.00mm (W) x 2.15mm (H)

View Direction	Diagram
Top	
Bottom	

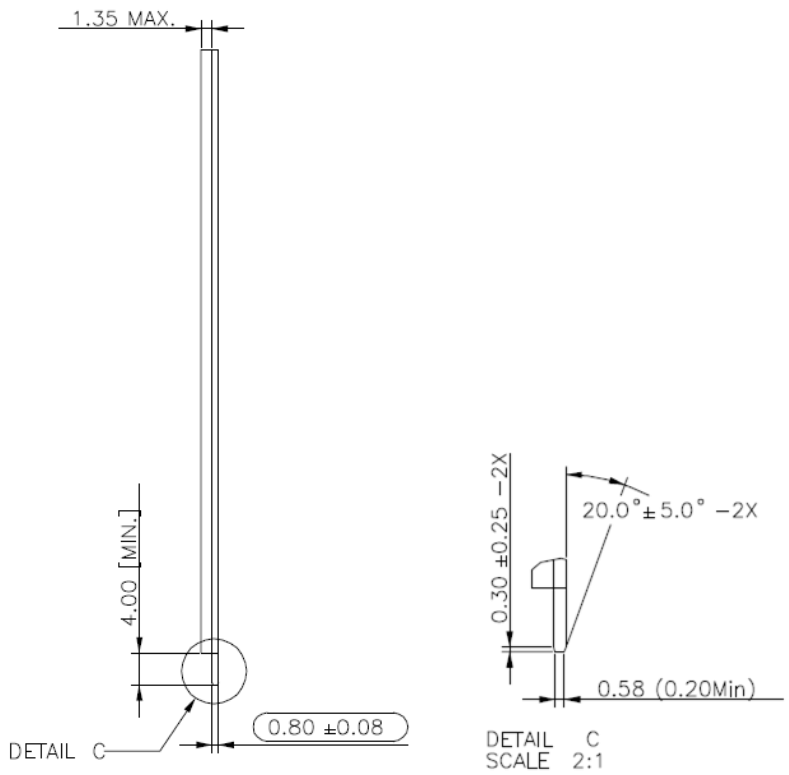
View Direction	Diagram
Side	
	Notes : 1. = Max Component Height 2. = No Component 3. = No Component / Signal Vias / Signal Copper / Printing 4.General Tolerance ±0.15mm 5. are critical dimensions

Figure 7-1 Product Mechanical Diagram and Dimensions

8. APPLICATION NOTES

8.1. Wafer Level Chip Scale Packaging (WLCSP) Handling Precautions

There are a lot of components assembled on a single SSD device. Please handle the drive with care especially when it has any WLCSP (Wafer Level Chip Scale Packaging) components such as PMIC, thermal sensor or load switch. WLCSP is one of the packaging technologies that is widely adopted for making smaller footprints, but any bumps or scratches may damage those ultra-small parts so gentle handling is strongly recommended.

⚠ DO NOT DROP SSD

⚠ INSTALL SSD WITH CARE

⚠ STORE SSD IN A PROPER PACKAGE

8.2. M Key M.2 SSD Assembly Precautions

M Key M.2 SSD (Figure 1) is only compatible to M Key (Figure 2) socket. As shown in Use Case 2, misuse may cause severe damages to SSD including burn-out.

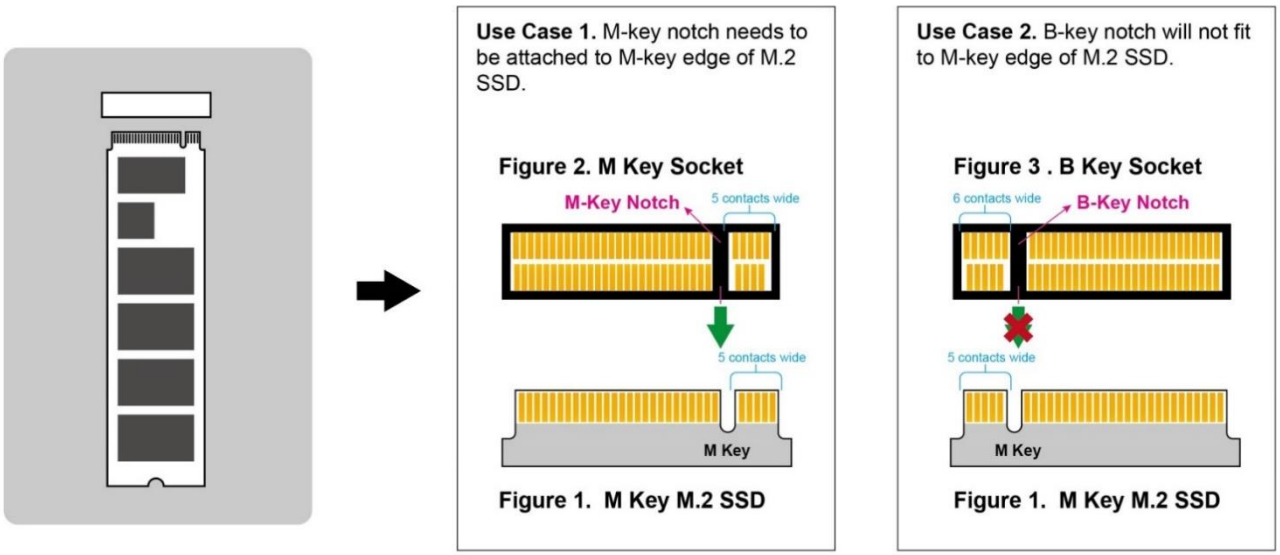


Figure 8-1 M Key M.2 Assembly Precautions

10. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 10-1 List of Terminology

Term	Definitions
ATTO	Commercial Performance Benchmark Application
DDR	Double Data Rate (SDRAM)
ASPM	Active States Power Management
APST	Autonomous Power State Transition
LBA	Logical Block Addressing
MB	Mega-Byte
GB	Giga-Byte
TB	Tera-Byte
MTBF	Mean Time Between Failures
PCIe	PCI Express / Peripheral Component Interconnect Express
S.M.A.R.T.	Self-Monitoring, Analysis and Reporting Technology
SSD	Solid State Disk

11. PRODUCT WARRANTY POLICY

In the event the Product does not conform to the specification within Abacus agreed warranty period and such inconformity is solely attributable to Phison's cause, Abacus agrees at its discretion replace or repair the nonconforming Product. Notwithstanding the foregoing, the aforementioned warranty shall exclude the inconformity arising from, in relation to or associated with:

(1) alternation, modification, improper use, misuse or excessive use of the Product;

(2) failure to comply with Abacus's instructions;

(3) Phison's compliance with customer (including customer's suppliers, subcontractors or downstream customers) indicated instructions, technologies, designs, specifications, materials, components, parts;

(4) combination of the Product with other materials, components, parts, goods, hardware, firmware or software not developed by Abacus; or

(5) other error or failure not solely attributable to Phison's cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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