DDR4-1.20V

SO DIMM Module

16GB based on 8Gb E-die

FBGA with Pb-Free

Revision 1.0(Feb 2024)

1.0 Feature

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP - 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 3.6V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 Bank with x8
- 8 Bank with x16
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or dif-ferent bank group accesses are available
- Data transfer rates: PC4-3200, PC4-2933, PC4-2666, PC4-2400, PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD for ECC SODIMM
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
ZH4G7S8EXN	16GB	2Gx64	1Gx8 (H5AG38EXNDX026N)*16	FBGA	2	16GB 2Rx8 PC4-3200S

3.0 Key Timing Parameters

	DDR4-3200	Unit
CL-tRCD-tRP	22-22-22	tCK
CAS Latency	22	tCK
tCK	0.625	ns
tRCD	13.75	ns
tRP	13.75	ns
tRAS	32	ns
tRC	47.0	ns

*SK hynix DRAM devices support optional downbinning to CL22, CL21, CL19, CL17, CL15, CL13 and CL11. SPD setting is programmed to match.

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
Vin , Vout	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V
V_{DD}	Voltage on V_{DD} relative to V_{ss}	-0.3 ~ 1.5	V
V_{DDQ}	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V
V_{PP}	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Front
1	VSS	2	VSS	65	VSS	66	DQ28
3	DQ5	4	DQ4	67	DQ29	68	VSS
5	VSS	6	VSS	69	VSS	70	DQ24
7	DQ1	8	DQ0	71	DQ25	72	VSS
9	VSS	10	VSS	73	VSS	74	DQS3_c
11	DQS0_c	12	DM0_n,DBI0_n	75	DM3_n,DBI3_n	76	DQS3_t
13	DQS0_t	14	VSS	77	VSS	78	VSS
15	VSS	16	DQ6	79	DQ30	80	DQ31
17	DQ7	18	VSS	81	VSS	82	VSS
19	VSS	20	DQ2	83	DQ26	84	DQ27
21	DQ3	22	VSS	85	VSS	86	VSS
23	VSS	24	DQ12	87	CB5,NC	88	CB4,NC
25	DQ13	26	VSS	89	VSS	90	VSS
27	VSS	28	DQ8	91	CB1,NC	92	CB0,NC
29	DQ9	30	VSS	93	VSS	94	VSS
31	VSS	32	DQS1_c	95	DQS8_c	96	DM8_n,DBI8_n
33	DM1_n,DBI1_n	34	DQS1_t	97	DQS8_c	98	VSS
35	VSS	36	VSS	99	VSS	100	CB6,NC
37	DQ15	38	DQ14	101	CB2,NC	102	VSS
39	VSS	40	VSS	103	VSS	104	CB7,NC
41	DQ10	42	DQ11	105	CB3,NC	106	VSS
43	VSS	44	VSS	107	VSS	108	RESET_n
45	DQ21	46	DQ20	109	CKE0	110	CKE1
47	VSS	48	VSS	111	VDD	112	VDD
49	DQ17	50	DQ16	113	BG1	114	ACT_n
51	VSS	52	VSS	115	BG0	116	ALERT_n
53	DQS2_c	54	DM2_n,DBI2_n	117	VDD	118	VDD
55	DQS2_t	56	VSS	119	A12	120	A11
57	VSS	58	DQ22	121	A9	122	A7
59	D123	60	VSS	123	VDD	124	VDD
61	VSS	62	DQ18	125	A8	126	A5
63	DQ19	64	VSS	127	A6	128	A4

Pin	Front	Pin	Front	Pin	Front	Pin	Front
129	VDD	130	VDD	137	CK0_t	138	CK1_t
131	A3	132	A2	139	CK0_c	140	CK1_c
133	A1	134	EVENT_n	141	VDD	142	VDD
135	VDD	136	VDD	143	PARITY	144	A0
145	BA1	146	A10/AP	203	DQ46	204	DQ47
147	VDD	148	VDD	205	VSS	206	VSS
149	CS0_n	150	BA0	207	DQ42	208	DQ43
151	A14/WE_n	152	A16/RAS_n	209	VSS	210	VSS
153	VDD	154	VDD	211	DQ52	212	DQ53
155	ODT0	156	A15/CAS_n	213	VSS	214	VSS
157	CS1_n	158	A13	215	DQ49	216	DQ48
159	VDD	160	VDD	217	VSS	218	VSS
161	ODT1	162	C0,CS2_n,NC	219	DQS6_c	220	DM6_n,DBI6_n
163	VDD	164	VREFCA	221	DQS6_t	222	VSS
165	C1,CS3_n,NC	166	SA2	223	VSS	224	DQ54
167	VSS	168	VSS	225	DQ55	226	VSS
169	DQ37	170	DQ36	227	VSS	228	DQ50
171	VSS	172	VSS	229	DQ51	230	VSS
173	DQ33	174	DQ32	231	VSS	232	DQ60
175	VSS	176	VSS	233	DQ61	234	VSS
177	DQS4_c	178	DM4_n,DBI4_n	235	VSS	236	DQ57
179	DQS4_t	180	VSS	237	DQ56	238	VSS
181	VSS	182	DQ39	239	VSS	240	DQS7_c
183	DQ38	184	VSS	241	DM7_n,DBI7_m	242	DQS7_t
185	VSS	186	DQ35	243	VSS	244	VSS
187	DQ34	188	VSS	245	DQ62	246	DQ63
189	VSS	190	DQ45	247	VSS	248	VSS
191	DQ44	192	VSS	249	DQ58	250	DQ59
193	VSS	194	DQ41	251	VSS	252	VSS
195	DQ40	196	VSS	253	SCL	254	SDA
197	VSS	198	DQS5_c	255	VDDSPD	256	SA0
199	DM5_n,DBI5_n	200	DQS5_t	257	VPP	258	VTT
201	VSS	202	VSS	259	VPP	260	SA1

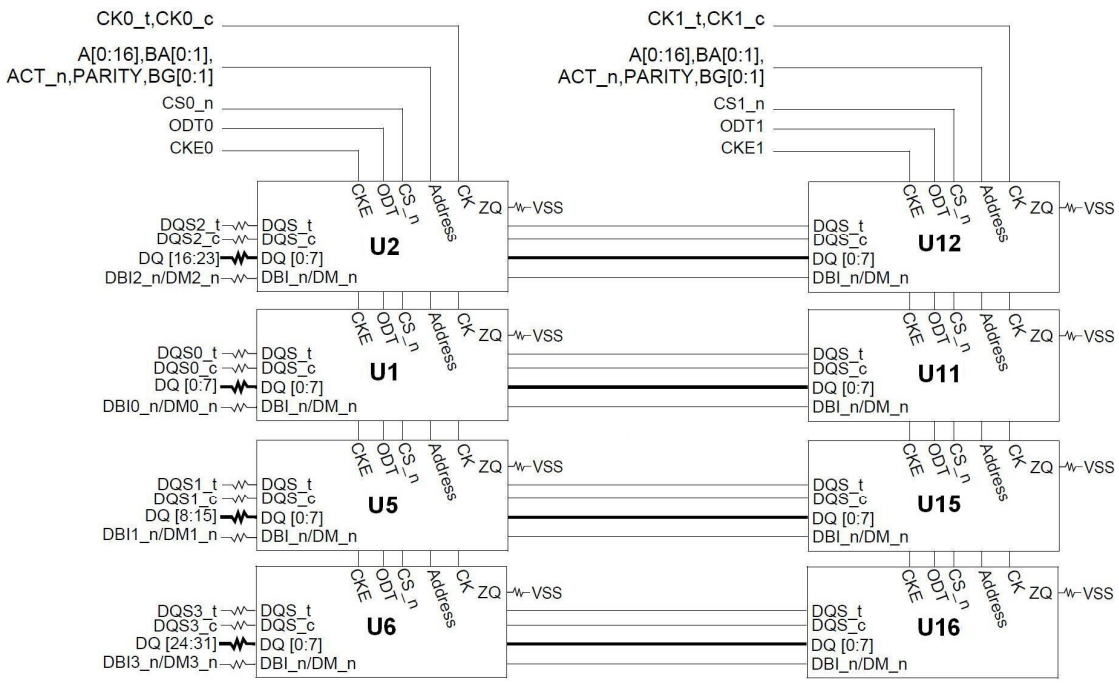
6.0 DIMM Pin Description

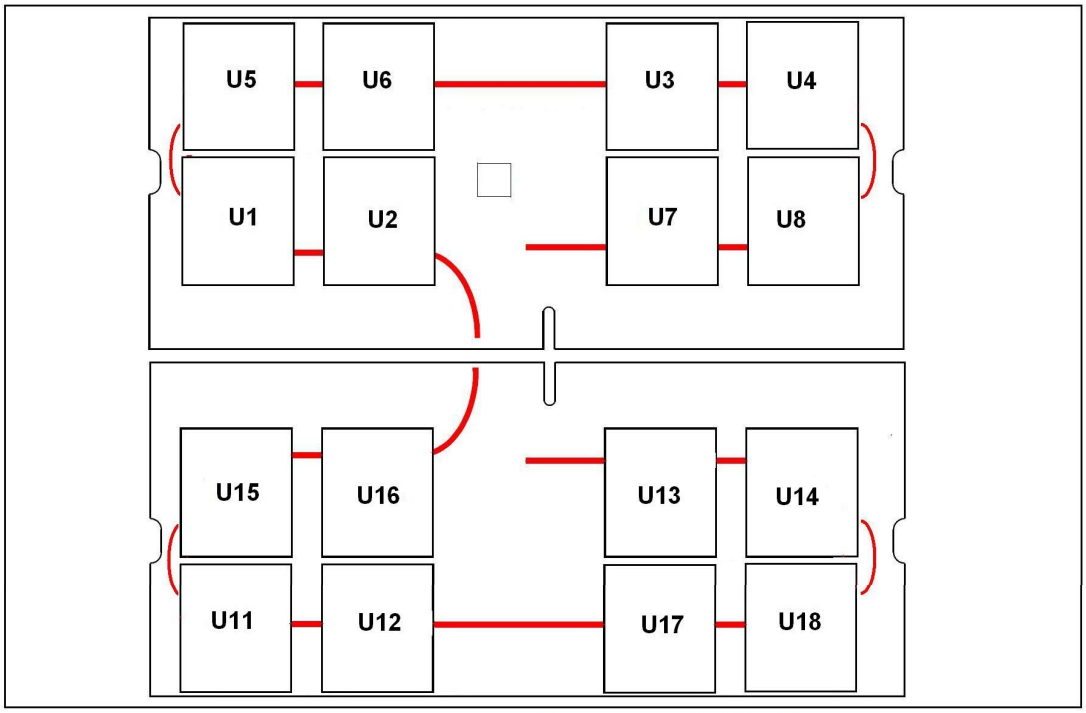
Pin Name	Function	Pin Name	Function
A0–A17	SDRAM address bus	SCL	I^2C serial bus clock for SPD-TSE
BA0–BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I^2C slave address select for SPD-TSE
RAS_n	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n	SDRAM column address strobe	VDD	SDRAM I/OO & core power supply
WE_n	SDRAM write enable	C0,C1,C2	Chip ID Lines
CS0_n,CS1_n	DIMM Rank Select Lines	12V	Optional power Supply on socket but not used on UDIMM
CKE0–CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM Activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n Output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply)
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)		
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to Known State
DM0_n–DM8_n DBI0_n–DBI8_n	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	EVENT_n	SPD signals a thermal event has occurred
CK0_t–CK1_t	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c–CK1_c	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

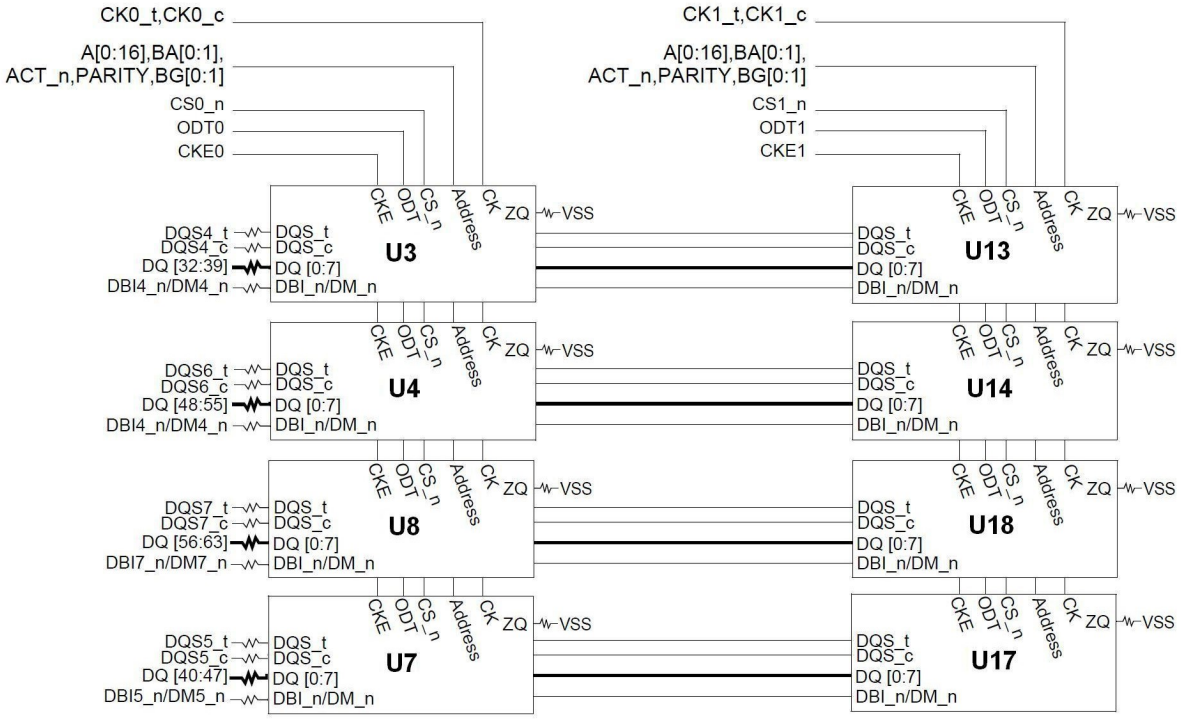
7.0 Address Configuration

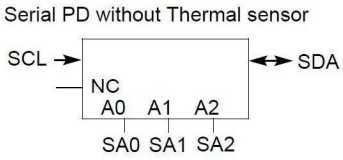
Organization	Bank Group Address	Row Address	Column Address	Bank Address	Page Size
2Gx64 (8Gb) base	BG0~BG01	A0-A15	A0-A9	BA0-BA1	1 KB

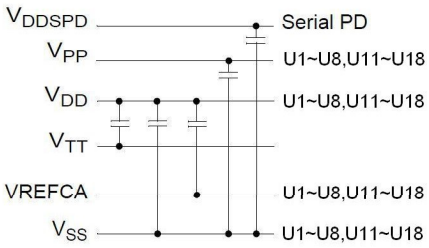
8.0 Functional Block Diagram: 16GB, 2Gx64 SO DIMM (Populated as 2 ranks ofx8)











9.0 AC & DC Operating Conditions

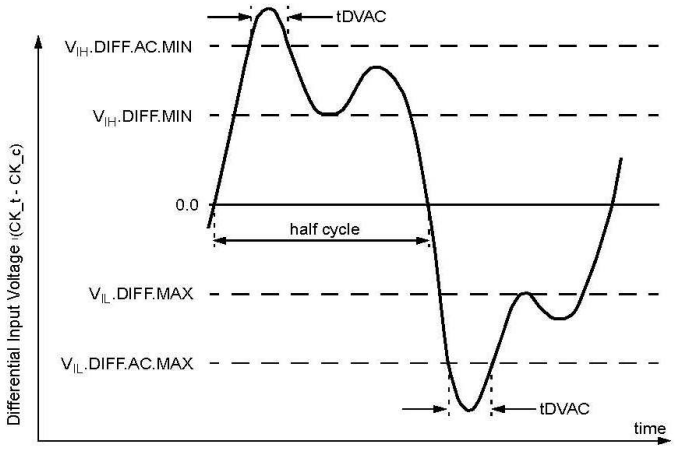
Recommended DC operating conditions

Symbol	Parameter	Min	Type	Max	Unit
VDD	Supply Voltage	1.14	1.20	1.26	V
VDDQ	Supply Voltage for Output	1.14	1.20	1.26	V
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V

10.1 AC and DC Input Levels for Single-Ended Signals

Symbol	Parameter	DDR4-3200		Unit
		Min	Max	
$V_{IH.CA}^{(DC75)}$	DC input logic high	$VREFCA^{+}$ 0.065	VDD	V
$V_{IL.CA}^{(DC75)}$	DC input logic low	VSS	$VREFCA^{-}$ 0.065	V
$V_{IH.CA}^{(AC100)}$	AC input logic high	$VREF^{+0.09}$	-	V
$V_{IL.CA}^{(AC100)}$	AC input logic low	-	$VREF^{-0.09}$	V
$VREFCA^{(DC)}$	Reference Voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	V

AC and DC Logic Input Levels for Differential Signals
Differential signal definition



NOTE:

1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

Definition of differential ac-swing and "time above ac-level" t_{DVAC}

10.2 Vref Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages VREFCA is illustrated in Figure below. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA). VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD.

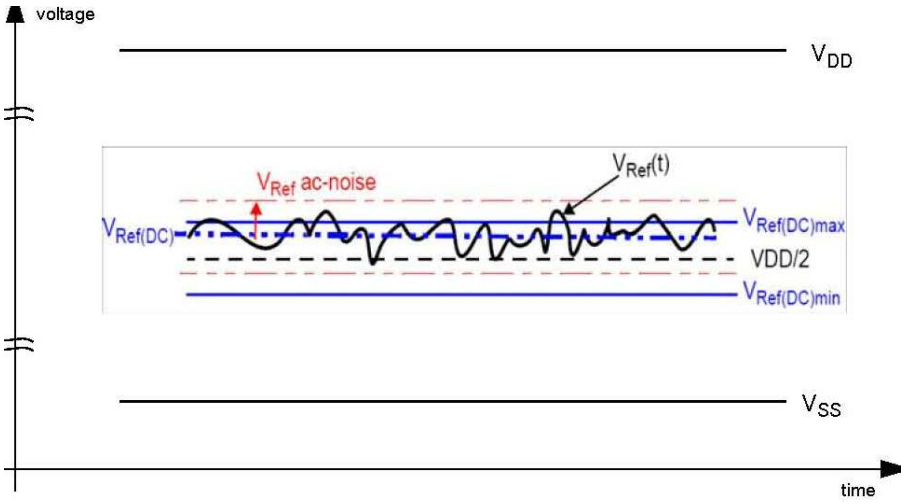


Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

11.0 IDD Specifications

Symbol	Condition	IDD	Unit
IDD0	Operating One Bank Active-Precharge Current	504	mA
IDD0A	Operating One Bank Active-Precharge Current	504	mA
IDD1	Operating One Bank Active-Read-Precharge Current	567	mA
IDD1A	Operating One Bank Active-Read-Precharge Current	596	mA
IDD2N	Precharge Standby Current	426	mA
IDD2NA	Precharge Standby Current	427	mA
IDD2NT	Precharge Standby ODT Current	499	mA
IDD2NL	Precharge Standby Current with CAL enabled	259	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled	418	mA
IDD2ND	Precharge Standby Current with DLL disabled	388	mA
IDD2NP	Precharge Standby Current with CA parity enabled	446	mA
IDD2P	Precharge Power-Down Current CKE	245	mA
IDD2Q	Precharge Quiet Standby Current	392	mA
IDD3N	Active Standby Current	721	mA
IDD3NA	Active Standby Current	721	
IDD3P	Active Power-Down Current	570	mA

Symbol	Condition	IDD	Unit
IDD4R	Operating Burst Read Current	1176	mA
IDD4RA	Operating Burst Read Current	1202	mA
IDD4RB	Operating Burst Read Current with Read DBI	1195	mA
IDD4W	Operating Burst Write Current	1121	mA
IDD4WA	Operating Burst Write Current	1161	mA
IDD4WB	Operating Burst Write Current with Write DBI	1066	mA
IDD4WC	Operating Burst Write Current with Write CRC	1114	mA
IDD4WP	Operating Burst Write Current with CA Parity	1187	mA
IDD5B	Burst Refresh Current	2232	mA
IDD5F2	Burst Refresh Current (2X REF)	1646	mA
IDD5F4	Burst Refresh Current (4X REF)	1417	mA
IDD6N	Self-Refresh Current: Normal Temperature Range	263	mA
IDD6E	Self-Refresh Current: Extended Temperature Range	441	mA
IDD6R	Self-Refresh Current: Reduced Temperature Range	120	mA
IDD6A	Auto Self-Refresh Current	442	mA
IDD7	Operating Bank Interleave Read Current	1304	mA
IDD8	Maximum Power Down Current	75	mA
IDD9		4780	mA

12.0 Standard Speed Bins

DDR4 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin

Speed Bin				DDR4-3200AA		Unit	NOTE
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75	-	ns	12
PRE command period			tRP	13.75	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.75	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,10
CWL = 12.16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 21	CL = 25	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.682	<0.75	ns	1,2,3
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.682	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.682	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22, 24		nCK	
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,25 26, 28		nCK	
Supported CWL Settings				9,10,11,12,14,16, 18,20		nCK	

Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400, 2933 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corre-sponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory fea-ture. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
12. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
13. DDR4-2400,2666,2933 and 3200Mbps speed bin support CL=10 if DRAM operate at 1333MT/s data rate.
14. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
15. CL number in parentheses, it means that these numbers are optional.
16. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
17. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

13.0 Environmental Parameters

Symbol	Parameter	Rating	Units
T_{OPR}	Operating temperature (ambient)	0 to +85	^{o}C
H_{OPR}	Operating humidity (relative)	10 to 90	%
T_{STG}	Storage temperature	-50 to +100	^{o}C
H_{STG}	Storage humidity (without condensation)	5 to 95	%
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal

14.0 Physical Dimensions: (1Gx8 Based, 2Gx64, 2 Ranks)