DDR5-1.10V

SO DIMM Module

32 GB based on 16Gbit component

FBGA with Pb-Free

Revision 1.0 (Dec,2023)

1.0 Feature

- DRAM VDD/VDDQ = 1.1V (-33mV / +67mV)
- DRAM VPP = 1.8V (–54mV / +108mV)
- 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Temperature Encoding
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Package Output Driver Test Mode• This product is in Compliance with the RoHS directive
- DIMM Dimension (Nominal) 30.00 mm high, 69.6 mm wide
- Based on JEDEC standard
- RoHS compliant & Halogen Free
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
ZHMCG88AGBS092Y1	32GB	4Gx64	2Gx8 (H5CG48AGBDX018N)*16	FBGA	2	32GB 2Rx8 PC5-5600S

3.0 Key Timing Parameters

	DDR5-5600	Unit
CL-tRCD-tRP	40-39-39	tCK
CAS Latency	16	tCK
tCK	0.357	ns
tRCD	16.00	ns
tRP	16.00	ns
tRAS	32.00	ns
tRC	48.00	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V
VIN, VOUT	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V
TSTG	Storage Temperature	-55 ~ + 100	°C

5.0 Address Configuration

Organization	Bank Group Address	Row Address	Column Address	Bank Address	Page Size
4Gx64 (16 Gb) base	BG0~BG2	R0-R15	C0-C9	BA0-BA1	1 KB

6.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VIN_BULK	2	HSA	97	VSS	98	VSS	191	DQ4_B	192	VSS
3	VIN_BULK	4	HSCL	99	CB2_A	100	DQS4_A_c	193	VSS	194	DQ5_B
5	RFU	6	HSDA	101	VSS	102	DQS4_A_t	195	DQ6_B	196	VSS
7	PWR_GOOD	8	PWR_EN	103	CB3_A	104	VSS	197	VSS	198	DQ7_B
9	VSS	10	VSS	105	VSS	106	CS0_A_n	199	DQ8_B	200	VSS
11	DQ0_A	12	DQ1_A	107	CA0_A	108	ALERT_n	201	VSS	202	DQ9_B
13	VSS	14	VSS	109	CA1_A	110	CS1_A_n	203	DQ10_B	204	VSS
15	DQ2_A	16	DQ3_A	111	VSS	112	VSS	205	VSS	206	DQ11_B
17	VSS	18	VSS	113	CA2_A	114	CA3_A	207	DQS1_B_c	208	VSS
19	DM0_A_n	20	DQS0_A_c	115	CA4_A	116	CA5_A	209	DQS1_B_t	210	DM1_B_n
21	VSS	22	DQS0_A_t	117	VSS	118	VSS	211	VSS	212	VSS
23	DQ4_A	24	VSS	119	CA6_A	120	CA7_A	213	DQ12_B	214	DQ13_B
25	VSS	26	DQ5_A	121	CA8_A	122	CA9_A	215	VSS	216	VSS
27	DQ6_A	28	VSS	123	VSS	124	VSS	217	DQ14_B	218	DQ15_B

262-Pin SO DIMM DDR5 SDRAM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
29	VSS	30	DQ7_A	125	CA10_A	126	CA11_A	219	VSS	220	VSS
31	DQ8_A	32	VSS	KEY				221	DQ16_B	222	DQ17_B
33	VSS	34	DQ09_A	127	CA12_A	128	RFU	223	VSS	224	VSS
35	DQ10_A	36	VSS	129	VSS	130	VSS	225	DQ18_B	226	DQ19_B
37	VSS	38	DQ11_A	131	CK0_A_t	132	CK1_A_t	227	VSS	228	VSS
39	DQS1_A_c	40	VSS	133	CK0_A_c	134	CK1_A_c	229	DM2_B_n	230	DQS2_B_c
41	DQS1_A_t	42	DM1_A_n	135	VSS	136	VSS	231	VSS	232	DQS2_B_t
43	VSS	44	VSS	137	CK0_B_t	138	CK1_B_t	233	DQ20_B	234	VSS
45	DQ12_A	46	DQ13_A	139	CK0_B_c	140	CK1_B_c	235	VSS	236	DQ21_B
47	VSS	48	VSS	141	VSS	142	VSS	237	DQ22_B	238	VSS
49	DQ14_A	50	DQ15_A	143	RFU	144	CA12_B	239	VSS	240	DQ23_B
51	VSS	52	VSS	145	CA11_B	146	CA10_B	241	DQ24_B	242	VSS
53	DQ16_A	54	DQ17_A	147	VSS	148	VSS	243	VSS	244	DQ25_B
55	VSS	56	VSS	149	CA9_B	150	CA8_B	245	DQ26_B	246	VSS
57	DQ18_A	58	DQ19_A	151	CA7_B	152	CA6_B	247	VSS	248	DQ27_B
59	VSS	60	VSS	153	VSS	154	VSS	249	DQS3_B_c	250	VSS
61	DM2_A_n	62	DQS2_A_c	155	CA5_B	156	CA4_B	251	DQS3_B_t	252	DM3_B_n
63	VSS	64	DQS2_A_t	157	CA3_B	158	CA2_B	253	VSS	254	VSS
65	DQ20_A	66	VSS	159	VSS	160	VSS	255	DQ28_B	256	DQ29_B
67	VSS	68	DQ21_A	161	CS0_B_n	162	CA1_B	257	VSS	258	VSS
69	DQ22_A	70	VSS	163	RESET_n	164	CA0_B	259	DQ30_B	260	DQ31_B
71	VSS	72	DQ23_A	165	CS1_B_n	166	VSS	261	VSS	262	VSS
73	DQ24_A	74	VSS	167	VSS	168	CB0_B				
75	VSS	76	DQ25_A	169	DQS4_B_c	170	VSS				
77	DQ26_A	78	VSS	171	DQS4_B_t	172	CB1_B				
79	VSS	80	DQ27_A	173	VSS	174	VSS				
81	DQS3_A_c	82	VSS	175	CB3_B	176	CB2_B				
83	DQS3_A_t	84	DM3_A_n	177	VSS	178	VSS				
85	VSS	86	VSS	179	DQ0_B	180	DQ1_B				
87	DQ28_A	88	DQ29_A	181	VSS	182	VSS				
89	VSS	90	VSS	183	DQ2_B	184	DQ3_B				
91	DQ30_A	92	DQ31_A	185	VSS	186	VSS				
93	VSS	94	VSS	187	DM0_B_n	188	DQS0_B_c				
95	CB0_A	96	CB1_A	189	VSS	190	DQS0_B_t				

7.0 DIMM Pin Description

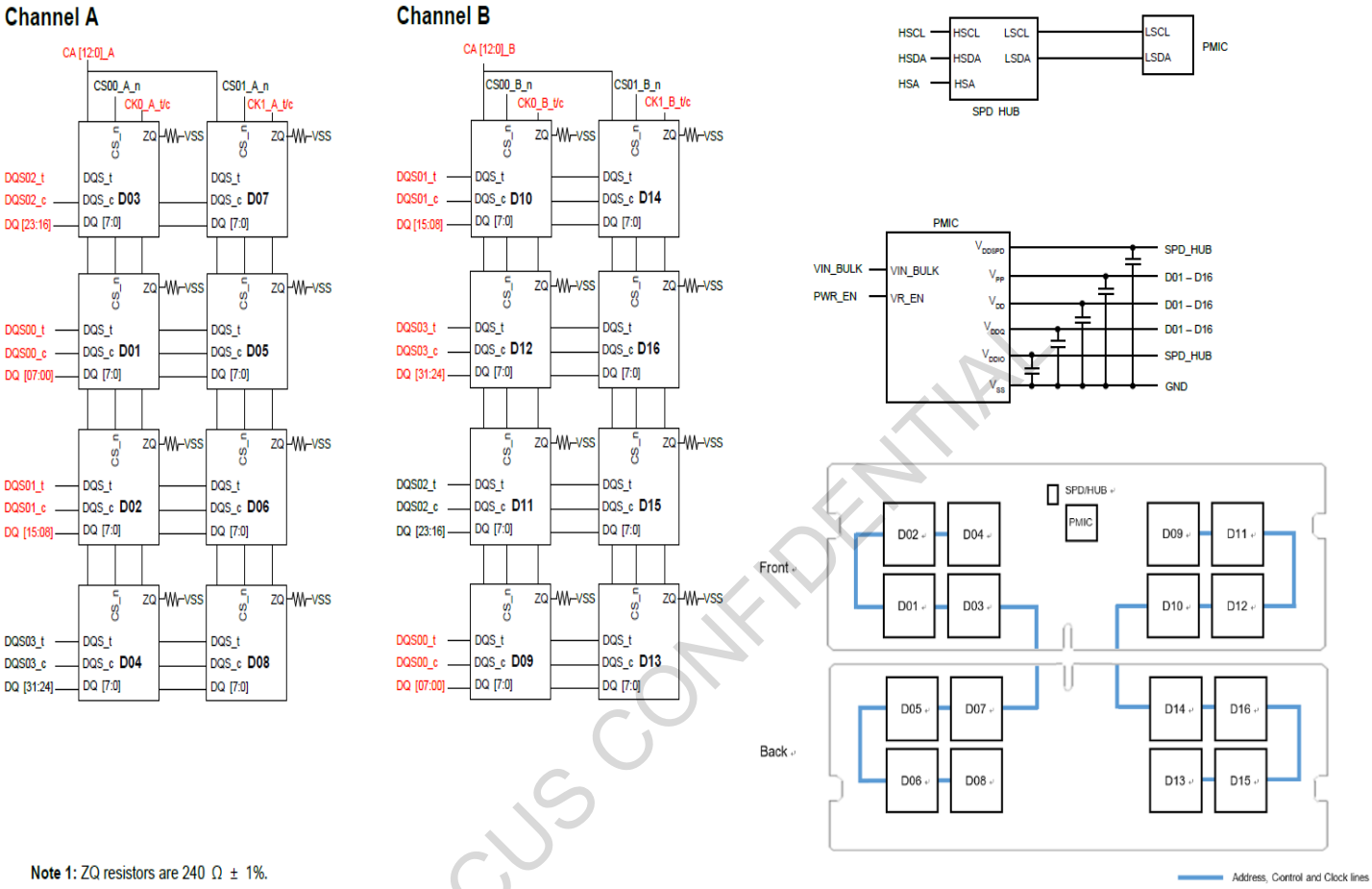
Pin Name	Function	Pin Name	Function
CA0_A - CA12_A	Command address input to channel A.	CA0_B - CA12_B	Command address input to channel B.
CS0_A_n - CS1_A_n	DIMM Rank Select Lines input for channel A.	CS0_B_n - CS1_B_n	DIMM Rank Select Lines input for channel B.
DQ0_A - DQ31_A	DIMM memory data bus for	DQ0_B - DQ31_B	DIMM memory data bus for
CB0_A - CB3_A	DIMM ECC check bits for channel A.	CB0_B - CB3_B	DIMM ECC check bits for channel B.
CK0_A_t, CK1_A_t	SDRAM clock for channel A. (positive line of differential pair)	CK0_B_t, CK1_B_t	SDRAM clock for channel B. (positive line of differential pair)
CK0_A_c, CK1_A_c	SDRAM clock for channel A. (negative line of differential pair)	CK0_B_c, CK1_B_c	SDRAM clock for channel B. (negative line of differential pair)
DQS0_A_t - DQS4_A_t	Data Buffer data strobes in channel A.(positive line of differential pair)	DQS0_B_t - DQS4_B_t	Data Buffer data strobes in channel B (positive line of differential
DQS0_A_c - DQS4_A_c	Data Buffer data strobes in channel A.(negative line of differential pair)	DQS0_B_c - DQS4_B_c	Data Buffer data strobes in channel
DM0_A_n - DM3_A_n	SDRAM input data mask signal for write data of channel A.	DM0_B_n- DM3_B_n	SDRAM input data mask signal for write data of channel B.
VIN_BULK	5 V power input supply pin to the PMIC.	VSS	Power supply return (ground)
PWR_GOOD	Output for Power good indicator from the PMIC. The PMIC ensures this pin high when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. Otherwise PMIC will drive this pin low. The PMIC disables its output regulator when this pin is low	PWR_EN	Power Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator.
HSCL	Side-band bus serial bus clock for SPDHub.	RESET_n	Set Register and SDRAMs to a Known State
HSDA	Side-band bus serial data line for SPDHub.	ALERT_n	Register ALERT_n output
HSA	Side-band bus Host ID and Hub device type ID selection.	RFU	Reserved for future use

8.0 Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA6_A, CA0_B - CA6_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
PAR_A PAR_B		
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input	DIMM ECC check bits
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
LBDQ	Output	Loopback Data Output: The Output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0]
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HIZ based on MR36:OP[2:0]

Symbol	Type	Function
ALERT_n	Input/ Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	Host SidebandBus bus clock, supplied by the master.
HSDA	Input/ Output	Host SidebandBus data, connected from the master to bubs or host bus client devices.
HSA	Input	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C Basic address range.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
PWR_EN	Input	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
PWR_GOOD	Input/ Output	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
VIN_BULK	Supply	5V power input supply to the PMIC for analog circuits.
VSS	Supply	Ground

9.0 Functional Block Diagram: 32 GB, 4Gx64 Module (Populated as 2 Rank ofx8)



Note 1: ZQ resistors are 240 Ω ± 1%.

10.0 AC & DC Operating Conditions

Recommended DC operating conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz	
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm

11.0 IDD Specifications

I D		
Symbol	**5600**	**Unit**
IDD0	273.4	mA
IDD0F	359.4	mA
IDD2N	241.2	mA
IDD2P	217.6	mA
IDD3N	361.0	mA
IDD3P	336.5	mA
IDD4R	840.8	mA
IDD4W	999.5	mA
IDD5B	697.2	mA
IDD5F	666.9	mA
IDD5C	429.8	mA
IDD6N	235.0	mA
IDD7	1048.50	mA
IDD8	104.6	mA
IDD9	468.0	mA

Module IDD is based on PMIC 5V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, current and PMIC efficiency.

12.0 Standard Speed Bins

Speed Bin	**Symbol**	**DDR5-5600B**		**Unit**
CL-nRCD-nRP		**46-45-45**		
Parameter		**min**	**max**	
Internal read command to first data	tAA	16.000	22.222	ns
ACT to internal read or write delay time	tRCD	16.000		ns
Row Precharge Time	tRP	16.000		ns
ACT to PRE command period	tRAS	32.00	5 x tREFI1	ns
ACT to ACT or REF command period	tRC	48.000		ns
CAS Write Latency	CWL	CWL=CL-2 (38)		ns

Speed Bin	tAAmin| (ns)	tRCDmin tRPmin (ns)	Read CL	Supported Frequency Down Bins			
	20.952	-	22	tCK(AVG)	0.952	1.010	ns
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	ns
3200BN 3200B	16.250	16.250	26	tCK(AVG)	0.625	0.681	ns
3200AN	15.000	15.000	24	tCK(AVG)	RESERVED		ns
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	ns
3600BN 3600B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	ns
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED		ns
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	ns
4000BN 4000B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	ns
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED		ns
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	ns
4400BN 4400B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	ns
4400AN	14.545	14.545	32	tCK(AVG)	RESERVED		ns
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	ns
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	ns

4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	ns
4800AN	14.166	14.166	34	tCK(AVG)	RESERVED		ns
5200C	17.692	17.692	46	tCK(AVG)	0.384	<0.416	ns
5200BN,B	16.153	16.153	42	tCK(AVG)	0.384	<0.416	ns
5200AN	14.615	14.615	38	tCK(AVG)	RESERVED		ns
5600C	17.857	17.500	50	tCK(AVG)	0.357	<0.384	ns
5600BN	16.428	16.428	46	tCK(AVG)	0.357	<0.384	ns
5600B	16.428	16.071	46	tCK(AVG)	0.357	<0.384	ns
5600AN	14.285	14.285	40	tCK(AVG)	RESERVED		ns
Supported CL					22,26,28,30,32,36,40,42,46,50		nCK

13.0 Environmental Parameters

Symbol	Parameter	Rating	Units
T_{OPR}	Operating temperature (ambient)	0 to +85	^oC
H_{OPR}	Operating humidity (relative)	10 to 90	%
T_{STG}	Storage temperature	-55 to +100	^oC
H_{STG}	Storage humidity (without condensation)	5 to 95	%
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal

14.0 Physical Dimensions: (2Gx8 Based, 4Gx64, 2 Ranks)