

DDR4-1.20V
Unbuffered DIMM Module

8GB based on 8Gb E-die

FBGA with Pb-Free



Revision 1.0(Feb,2024)

1.0 Feature

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP - 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 3.6V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 Bank with x8
- 8 Bank with x16
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or dif-ferent bank group accesses are available
- Data transfer rates: PC4-3200, PC4-2933, PC4-2666, PC4-2400, PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD for ECC UDIMM
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available

2.0 Ordering Information

| Part number | Density | Module Organization | Component composition | Component PKG | Module Rank | Description |
|-------------|---------|---------------------|-----------------------------|---------------|-------------|--------------------|
| ZH4G6U8EXN | 8GB | 1Gx64 | 1Gx8 (H5AG38EXNDX026N)*8 | FBGA | 1 | 8GB 1Rx8 PC4-3200U |

3.0 Key Timing Parameters

| | DDR4-3200 | Unit |
|-------------|-----------|------|
| CL-tRCD-tRP | 22-22-22 | tCK |
| CAS Latency | 22 | tCK |
| tCK | 0.625 | ns |
| tRCD | 13.75 | ns |
| tRP | 13.75 | ns |
| tRAS | 32 | ns |
| tRC | 47.0 | ns |

*SK hynix DRAM devices support optional downbinning to CL22, CL21, CL19, CL17, CL15, CL13 and CL11. SPD setting is pro-grammed to match.

4.0 Absolute Maximum DC Rating

| Symbol | Parameter | Rating | Units |
|------------------------------------|--|-------------|-------|
| V _{in} , V _{out} | Voltage on any pin except VREFCA relative to V _{ss} | -0.3 ~ 1.5 | V |
| VDD | Voltage on VDD relative to V _{ss} | -0.3 ~ 1.5 | V |
| VDDQ | Voltage on VDD pin relative to V _{ss} | -0.3 ~ 1.5 | V |
| VPP | Voltage on VPP pin relative to V _{ss} | -0.3 ~ 3.0 | V |
| TSTG | Storage Temperature | -55 ~ + 100 | °C |

5.0 DIMM Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|-------|-----|--------|-----|-------|-----|---------|
| 1 | NC | 145 | NC | 33 | VSS | 177 | DQ23 |
| 2 | VSS | 146 | VREFCA | 34 | DQ18 | 178 | VSS |
| 3 | DQ04 | 147 | VSS | 35 | VSS | 179 | DQ19 |
| 4 | VSS | 148 | DQ05 | 36 | DQ28 | 180 | VSS |
| 5 | DQ00 | 149 | VSS | 37 | VSS | 181 | DQ29 |
| 6 | VSS | 150 | DQ01 | 38 | DQ24 | 182 | VSS |
| 7 | DM0_N | 151 | VSS | 39 | VSS | 183 | DQ25 |
| 8 | NC | 152 | DQS0_C | 40 | DM3_N | 184 | VSS |
| 9 | VSS | 153 | DQS0_T | 41 | NC | 185 | DQS3_C |
| 10 | DQ06 | 154 | VSS | 42 | VSS | 186 | DQS3_T |
| 11 | VSS | 155 | DQ07 | 43 | DQ30 | 187 | VSS |
| 12 | DQ02 | 156 | VSS | 44 | VSS | 188 | DQ31 |
| 13 | VSS | 157 | DQ03 | 45 | DQ26 | 189 | VSS |
| 14 | DQ12 | 158 | VSS | 46 | VSS | 190 | DQ27 |
| 15 | VSS | 159 | DQ13 | 47 | NC | 191 | VSS |
| 16 | DQ08 | 160 | VSS | 48 | VSS | 192 | NC |
| 17 | VSS | 161 | DQ09 | 49 | NC | 193 | VSS |
| 18 | DM1_N | 162 | VSS | 50 | VSS | 194 | NC |
| 19 | NC | 163 | DQS1_C | 51 | NC | 195 | VSS |
| 20 | VSS | 164 | DQS1_T | 52 | NC | 196 | NC |
| 21 | DQ14 | 165 | VSS | 53 | VSS | 197 | NC |
| 22 | VSS | 166 | DQ15 | 54 | NC | 198 | VSS |
| 23 | DQ10 | 167 | VSS | 55 | VSS | 199 | NC |
| 24 | VSS | 168 | DQ11 | 56 | NC | 200 | VSS |
| 25 | DQ20 | 169 | VSS | 57 | VSS | 201 | NC |
| 26 | VSS | 170 | DQ21 | 58 | RST_N | 202 | VSS |
| 27 | DQ16 | 171 | VSS | 59 | VDD | 203 | CKE1 |
| 28 | VSS | 172 | DQ17 | 60 | CKE0 | 204 | VDD |
| 29 | DM2_N | 173 | VSS | 61 | VDD | 205 | NC |
| 30 | NC | 174 | DQS2_C | 62 | ACT_N | 206 | VDD |
| 31 | VSS | 175 | DQS2_T | 63 | BG0 | 207 | BG1 |
| 32 | DQ22 | 176 | VSS | 64 | VDD | 208 | ALERT_N |

| Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|---------|-----|--------|-----|-------|-----|--------|
| 65 | A12 | 209 | VDD | 105 | VSS | 249 | DQ35 |
| 66 | A09 | 210 | A11 | 106 | DQ44 | 250 | VSS |
| 67 | VDD | 211 | A07 | 107 | VSS | 251 | DQ45 |
| 68 | A08 | 212 | VDD | 108 | DQ40 | 252 | VSS |
| 69 | A06 | 213 | A05 | 109 | VSS | 253 | DQ41 |
| 70 | VDD | 214 | A04 | 110 | DM5_N | 254 | VSS |
| 71 | A03 | 215 | VDD | 111 | NC | 255 | DQS5_C |
| 72 | A01 | 216 | A02 | 112 | VSS | 256 | DQS5_T |
| 73 | VDD | 217 | VDD | 113 | DQ46 | 257 | VSS |
| 74 | CK0_T | 218 | CK1_T | 114 | VSS | 258 | DQ47 |
| 75 | CK0_C | 219 | CK1_C | 115 | DQ42 | 259 | VSS |
| 76 | VDD | 220 | VDD | 116 | VSS | 260 | DQ43 |
| 77 | VTT | 221 | VTT | 117 | DQ52 | 261 | VSS |
| 78 | EVENT_N | 222 | PARITY | 118 | VSS | 262 | DQ53 |
| 79 | A00 | 223 | VDD | 119 | DQ48 | 263 | VSS |
| 80 | VDD | 224 | BA1 | 120 | VSS | 264 | DQ49 |
| 81 | BA0 | 225 | A10 | 121 | DM6_N | 265 | VSS |
| 82 | A16 | 226 | VDD | 122 | NC | 266 | DQS6_C |
| 83 | VDD | 227 | RFU | 123 | VSS | 267 | DQS6_T |
| 84 | CS0_N | 228 | A14 | 124 | DQ54 | 268 | VSS |
| 85 | VDD | 229 | VDD | 125 | VSS | 269 | DQ55 |
| 86 | A15 | 230 | NC | 126 | DQ50 | 270 | VSS |
| 87 | ODT0 | 231 | VDD | 127 | VSS | 271 | DQ51 |
| 88 | VDD | 232 | A13 | 128 | DQ60 | 272 | VSS |
| 89 | CS1_N | 233 | VDD | 129 | VSS | 273 | DQ61 |
| 90 | VDD | 234 | NC | 130 | DQ56 | 274 | VSS |
| 91 | ODT1 | 235 | NC | 131 | VSS | 275 | DQ57 |
| 92 | VDD | 236 | VDD | 132 | DM7_N | 276 | VSS |
| 93 | NC | 237 | NC | 133 | NC | 277 | DQS7_C |
| 94 | VSS | 238 | SA2 | 134 | VSS | 278 | DQS7_T |
| 95 | DQ36 | 239 | VSS | 135 | DQ62 | 279 | VSS |
| 96 | VSS | 240 | DQ37 | 136 | VSS | 280 | DQ63 |
| 97 | DQ32 | 241 | VSS | 137 | DQ58 | 281 | VSS |
| 98 | VSS | 242 | DQ33 | 138 | VSS | 282 | DQ59 |
| 99 | DM4_N | 243 | VSS | 139 | SA0 | 283 | VSS |
| 100 | NC | 244 | DQS4_C | 140 | SA1 | 284 | VDDSPD |
| 101 | VSS | 245 | DQS4_T | 141 | SCL | 285 | SDA |
| 102 | DQ38 | 246 | VSS | 142 | VPP | 286 | VPP |
| 103 | VSS | 247 | DQ39 | 143 | VPP | 287 | VPP |
| 104 | DQ34 | 248 | VSS | 144 | NC | 288 | VPP |

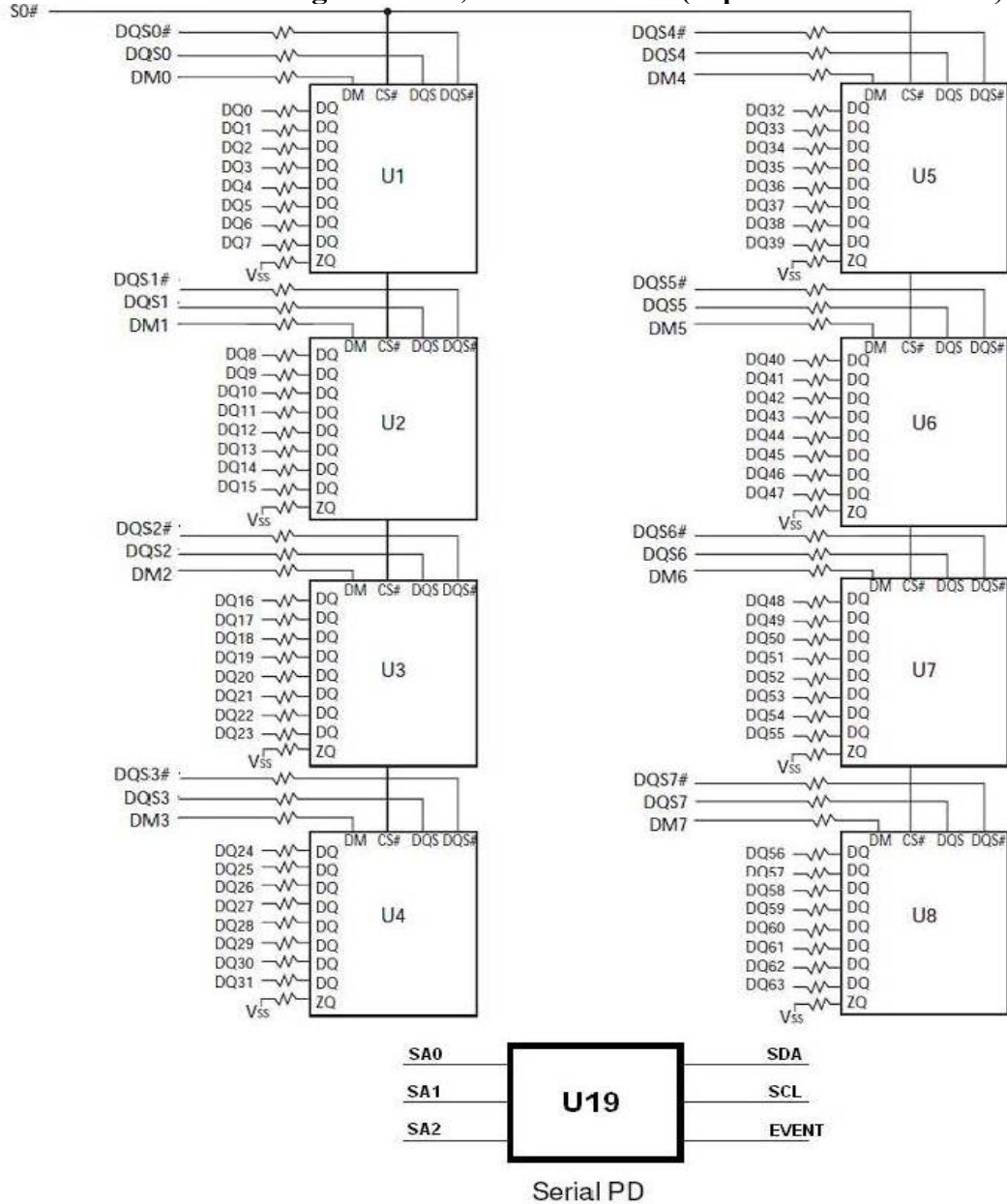
6.0 DIMM Pin Description

| Pin Name | Function | Pin Name | Function |
|--|--|--------------------|---|
| A0–A17 | SDRAM address bus | SCL | I ² C serial bus clock for SPD-TSE |
| BA0–BA1 | SDRAM bank select | SDA | I ² C serial bus data line for SPD-TSE |
| BG0, BG1 | SDRAM bank group select | SA0–SA2 | I ² C slave address select for SPD-TSE |
| RAS _n | SDRAM row address strobe | PARITY | SDRAM parity input |
| CAS _n | SDRAM column address strobe | VDD | SDRAM I/O & core power supply |
| WE _n | SDRAM write enable | C0,C1,C2 | Chip ID Lines |
| CS0 _n ,CS1 _n | DIMM Rank Select Lines | 12V | Optional power Supply on socket but not used on UDIMM |
| CKE0–CKE1 | SDRAM clock enable lines | VREFCA | SDRAM command/address reference supply |
| ODT0–ODT1 | On-die termination control lines | VSS | Power supply return (ground) |
| ACT _n | SDRAM Activate | VDDSPD | Serial SPD-TSE positive power supply |
| DQ0–DQ63 | DIMM memory data bus | ALERT _n | SDRAM ALERT _n Output |
| CB0–CB7 | DIMM ECC check bits | VPP | SDRAM Supply) |
| TDQS0 _t -TDQS8 _t TDQS0 _c -TDQS8 _c | Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs. | | |
| DQS0 _t -DQS8 _t | SDRAM data strobes (positive line of differential pair) | | |
| DQS0 _c -DQS8 _c | SDRAM data strobes (negative line of differential pair) | RESET _n | Set DRAMs to Known State |
| DM0 _n -DM8 _n DBI0 _n -DBI8 _n | SDRAM data masks/high data strobes (x8-based x72 DIMMs) | EVENT _n | SPD signals a thermal event has occurred |
| CK0 _t -CK1 _t | SDRAM clocks (positive line of differential pair) | VTT | SDRAM I/O termination supply |
| CK0 _c -CK1 _c | SDRAM clocks (negative line of differential pair) | RFU | Reserved for future use |

7.0 Address Configuration

| Organization | Bank Group Address | Row Address | Column Address | Bank Address | Page Size |
|------------------|--------------------|-------------|----------------|--------------|-----------|
| 1Gx64 (8Gb) base | BG0-BG01 | A0-A15 | A0-A9 | BA0-BA1 | 1 KB |

8.0 Functional Block Diagram: 8GB, 1Gx64 Module (Populated as 1 rank of x8)



9.0 AC & DC Operating Conditions

Recommended DC operating conditions

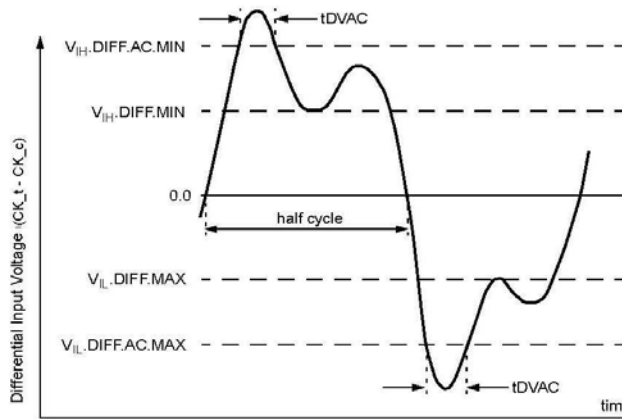
| Symbol | Parameter | Min | Type | Max | Unit |
|--------|------------------------------------|-------|------|------|------|
| VDD | Supply Voltage | 1.14 | 1.20 | 1.26 | V |
| VDDQ | Supply Voltage for Output | 1.14 | 1.20 | 1.26 | V |
| VPP | Supply Voltage for DRAM Activating | 2.375 | 2.5 | 2.75 | V |

10.1 AC and DC Input Levels for Single-Ended Signals

| Symbol | Parameter | DDR4-3200 | | Unit |
|---------------------------------------|--|------------------------------|------------------------------|------|
| | | Min | Max | |
| V _{IH,CA} ^(DC75) | DC input logic high | VREFCA ⁺ 0.065 | VDD | V |
| V _{IL,CA} ^(DC75) | DC input logic low | VSS | VREFCA ⁻ 0.065 | V |
| V _{IH,CA} ^(AC100) | AC input logic high | VREF ^{+0.09} | - | V |
| V _{IL,CA} ^(AC100) | AC input logic low | - | VREF ^{-0.09} | V |
| VREFCA ^(DC) | Reference Voltage for ADD, CMD inputs | 0.49*VDD | 0.51*VDD | V |

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



NOTE:

1. Differential signal rising edge from V_{IL,DIFF,MAX} to V_{IH,DIFF,MIN} must be monotonic slope.
2. Differential signal falling edge from V_{IH,DIFF,MIN} to V_{IL,DIFF,MAX} must be monotonic slope.

Definition of differential ac-swing and "time above ac-level" t_{DVAC}

10.2 Vref Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages VREFCA is illustrated in Figure below. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA). VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than $\pm 1\%$ VDD.

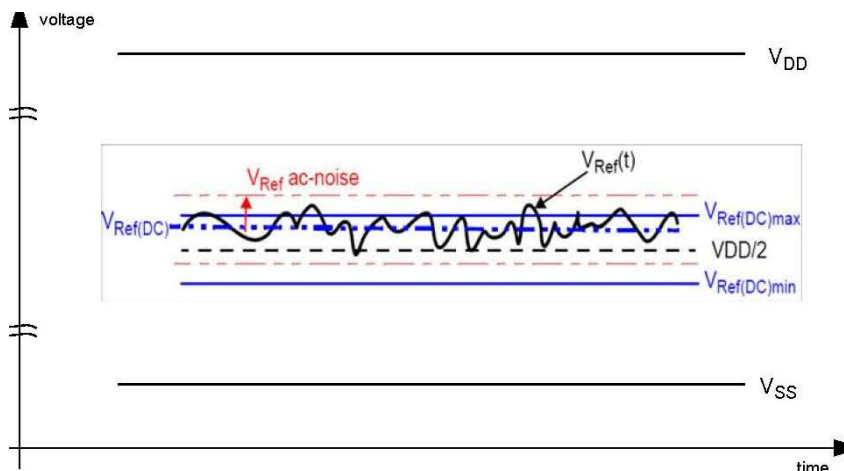


Illustration of $V_{REF(DC)}$ tolerance and V_{REF} AC-noise limits

11.0 IDD Specifications

| Symbol | Condition | IDD | Unit |
|--------|---|-----|------|
| IDD0 | Operating One Bank Active-Precharge Current□ | 292 | mA |
| IDD0A | Operating One Bank Active-Precharge Current□ | 292 | mA |
| IDD1 | Operating One Bank Active-Read-Precharge Current | 356 | mA |
| IDD1A | Operating One Bank Active-Read-Precharge Current | 385 | mA |
| IDD2N | Precharge Standby Current | 214 | mA |
| IDD2NA | Precharge Standby Current | 215 | mA |
| IDD2NT | Precharge Standby ODT Current | 251 | mA |
| IDD2NL | Precharge Standby Current with CAL enabled | 130 | mA |
| IDD2NG | Precharge Standby Current with Gear Down mode enabled | 210 | mA |
| IDD2ND | Precharge Standby Current with DLL disabled | 195 | mA |
| IDD2NP | Precharge Standby Current with CA parity enabled | 224 | mA |
| IDD2P | Precharge Power-Down Current CKE | 123 | mA |
| IDD2Q | Precharge Quiet Standby Current | 197 | mA |
| IDD3N | Active Standby Current | 363 | mA |
| IDD3NA | Active Standby Current | 363 | mA |
| IDD3P | Active Power-Down Current | 288 | mA |

| Symbol | Condition | IDD | Unit |
|--------|--|------|------|
| IDD4R | Operating Burst Read Current | 966 | mA |
| IDD4RA | Operating Burst Read Current | 992 | mA |
| IDD4RB | Operating Burst Read Current with Read DBI | 985 | mA |
| IDD4W | Operating Burst Write Current | 911 | mA |
| IDD4WA | Operating Burst Write Current | 950 | mA |
| IDD4WB | Operating Burst Write Current with Write DBI | 856 | mA |
| IDD4WC | Operating Burst Write Current with Write CRC | 904 | mA |
| IDD4WP | Operating Burst Write Current with CA Parity | 977 | mA |
| IDD5B | Burst Refresh Current | 2023 | mA |
| IDD5F2 | Burst Refresh Current (2X REF) | 1436 | mA |
| IDD5F4 | Burst Refresh Current (4X REF) | 1207 | mA |
| IDD6N | Self-Refresh Current: Normal Temperature Range | 132 | mA |
| IDD6E | Self-Refresh Current: Extended Temperature Range | 221 | mA |
| IDD6R | Self-Refresh Current: Reduced Temperature Range | 61 | mA |
| IDD6A | Auto Self-Refresh Current | 222 | mA |
| IDD7 | Operating Bank Interleave Read Current | 1093 | mA |
| IDD8 | Maximum Power Down Current | 38 | mA |
| IDD9 | | 2394 | mA |

12.0 Standard Speed Bins

DDR4 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin

| Speed Bin | | | DDR4-3200AA | | Unit | NOTE | |
|---|---------|----------|---|-----------------|--------|------|------------|
| CL-nRCD-nRP | | | 22-22-22 | | | | |
| Parameter | Symbol | | min | max | | | |
| Internal read command to first data | tAA | | 13.75 | 18.00 | ns | 12 | |
| Internal read command to first data with read DBI enabled | tAA_DBI | | tAA(min) + 4nCK | tAA(max) + 4nCK | ns | 12 | |
| ACT to internal read or write delay time | tRCD | | 13.75 | - | ns | 12 | |
| PRE command period | tRP | | 13.75 | - | ns | 12 | |
| ACT to PRE command period | tRAS | | 32 | 9 x tREFI | ns | 12 | |
| ACT to ACT or REF command period | tRC | | 45.75 | - | ns | 12 | |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | Reserved | | ns | 1,2,3,4,11 |
| | CL = 10 | CL = 12 | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,4,11 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,10 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,10 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,10 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,10 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,10 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,10 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | | ns | 1,2,3,4,10 |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3,4,10 |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3,10 |
| CWL = 14,18 | CL = 17 | CL = 20 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 18 | CL = 21 | tCK(AVG) | Reserved | | ns | 1,2,3,4,10 |
| | CL = 19 | CL = 22 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,4,10 |
| | CL = 20 | CL = 23 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,10 |
| CWL = 16,20 | CL = 20 | CL = 24 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 21 | CL = 25 | tCK(AVG) | 0.682 | <0.75 | ns | 1,2,3,4 |
| | CL = 22 | CL = 26 | tCK(AVG) | 0.682 | <0.75 | ns | 1,2,3,4 |
| | CL = 24 | CL = 28 | tCK(AVG) | 0.682 | <0.75 | ns | 1,2,3 |
| CWL = 16,20 | CL = 20 | CL = 24 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 22 | CL = 26 | tCK(AVG) | 0.625 | <0.682 | ns | 1,2,3,4 |
| | CL = 24 | CL = 28 | tCK(AVG) | 0.625 | <0.682 | ns | 1,2,3 |
| Supported CL Settings | | | 10,11,12,13,14,15,16,17,18,19,20,21,22,24 | | nCK | | |
| Supported CL Settings with read DBI | | | 12,13,14,15,16,18,19,20,21,22,23,25,26,28 | | nCK | | |
| Supported CWL Settings | | | 9,10,11,12,14,16,18,20 | | nCK | | |

Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V

- VPP = 2.5V +0.25/-0.125 V

- The values defined with above-mentioned table are DLL ON case.

- DDR4-1600, 1866, 2133, 2400, 2933 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

- The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
- tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
- 'Reserved' settings are not allowed. User must program a different value.
- 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
- Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
- DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
- DDR4-2400,2666,2933 and 3200Mbps speed bin support CL=10 if DRAM operate at 1333MT/s data rate.
- Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
- CL number in parentheses, it means that these numbers are optional.
- DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
- Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

13.0 Environmental Parameters

| Symbol | Parameter | Rating | Units |
|------------------|---|-------------|----------|
| T _{OPR} | Operating temperature (ambient) | 0 to +85 | °C |
| H _{OPR} | Operating humidity (relative) | 10 to 90 | % |
| T _{STG} | Storage temperature | -50 to +100 | °C |
| H _{STG} | Storage humidity (without condensation) | 5 to 95 | % |
| P _{BAR} | Barometric Pressure (operating & storage) | 105 to 69 | K Pascal |

14.0 Physical Dimensions: (1Gx8 Based, 1Gx64, 1 Rank)

