DDR4-1.20V

Unbuffered DIMM Module

8 GB based on 8Gbit component

FBGA with Pb-Free

Revision 5.4 (Aug,2022)
-Initial Release

288-Pin Unbuffered DIMM DDR4 SDRAM

1.0 Feature

- Power Supply: VDD=1.20V
- VPP=2.5V (NOM)
- VDDSPD=2.5V (NOM)
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- Data transfer rates: PC4-3200
- Single-rank
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- On-board I2C serial presence-detect (SPD) EEPROM
- On-die VREFDQ generation and calibration
- Selectable BC4 or BL8 on-the-fly (OTF)
- RoHS compliant & Halogen Free
- DIMM Dimension (Nominal) 31.25 mm high, 133.35 mm wide
- Fly-by topology
- Terminated control command and address bus
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
ZM4G6U8062ER	8GB	1Gx64	1Gx8 MT40A1G8SA-062E:R*8	FBGA	1	8GB 1Rx8 PC4-3200U

3.0 Key Timing Parameters

	DDR4-3200	Unit
CL-tRCD-tRP	22-22-22	tCK
CAS Latency	22	tCK
tCK	0.620	ns
tRCD	13.75	ns
tRP	13.75	ns
tRC	45.75	ns

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4.0 Address Configuration

Device configuration	Bank Group Address	Row Address	Column Address	Bank Address	Module Rank Address
1Gx8 (8Gb),16 Banks	4 BG[1:0]	64K A[15:0]	1K A[9:0]	4 BA[1:0]	CS0_n

5.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
Vin , Vout	Voltage on any pin relative to VSS	-0.4 ~ 1.5	V
V_{DD}	Voltage on V_{DD} relative to V_{ss}	-0.4 ~ 1.5	V
V_{DDQ}	Voltage on VDD pin relative to Vss	-0.4 ~ 1.5	V
V_{PP}	Voltage on VPP pin relative to Vss	-0.4 ~ 3.0	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

6.0 DIMM Pin Configurations (Front side/Back side)

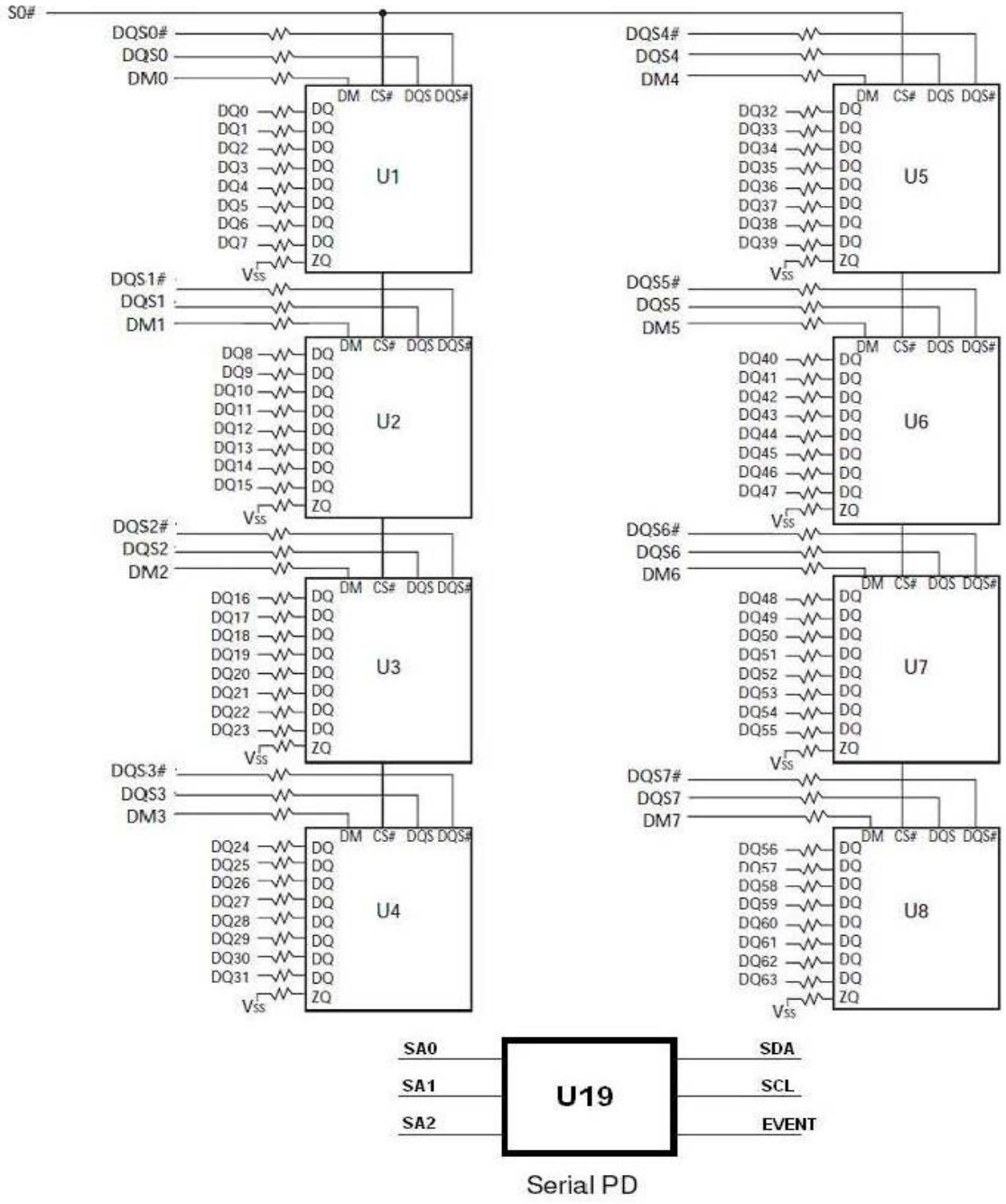
Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	33	VSS	177	DQ23
2	VSS	146	VREFCA	34	DQ18	178	VSS
3	DQ04	147	VSS	35	VSS	179	DQ19
4	VSS	148	DQ05	36	DQ28	180	VSS
5	DQ00	149	VSS	37	VSS	181	DQ29
6	VSS	150	DQ01	38	DQ24	182	VSS
7	DM0_N	151	VSS	39	VSS	183	DQ25
8	NC	152	DQS0_C	40	DM3_N	184	VSS
9	VSS	153	DQS0_T	41	NC	185	DQS3_C
10	DQ06	154	VSS	42	VSS	186	DQS3_T
11	VSS	155	DQ07	43	DQ30	187	VSS
12	DQ02	156	VSS	44	VSS	188	DQ31
13	VSS	157	DQ03	45	DQ26	189	VSS
14	DQ12	158	VSS	46	VSS	190	DQ27
15	VSS	159	DQ13	47	NC	191	VSS
16	DQ08	160	VSS	48	VSS	192	NC
17	VSS	161	DQ09	49	NC	193	VSS
18	DM1_N	162	VSS	50	VSS	194	NC
19	NC	163	DQS1_C	51	NC	195	VSS
20	VSS	164	DQS1_T	52	NC	196	NC
21	DQ14	165	VSS	53	VSS	197	NC
22	VSS	166	DQ15	54	NC	198	VSS
23	DQ10	167	VSS	55	VSS	199	NC
24	VSS	168	DQ11	56	NC	200	VSS
25	DQ20	169	VSS	57	VSS	201	NC
26	VSS	170	DQ21	58	RST_N	202	VSS
27	DQ16	171	VSS	59	VDD	203	CKE1
28	VSS	172	DQ17	60	CKE0	204	VDD
29	DM2_N	173	VSS	61	VDD	205	NC
30	NC	174	DQS2_C	62	ACT_N	206	VDD
31	VSS	175	DQS2_T	63	BG0	207	BG1
32	DQ22	176	VSS	64	VDD	208	ALERT_N

288-Pin Unbuffered DIMM DDR4 SDRAM

Pin	Front	Pin	Back	Pin	Front	Pin	Back
65	A12	209	VDD	105	VSS	249	DQ35
66	A09	210	A11	106	DQ44	250	VSS
67	VDD	211	A07	107	VSS	251	DQ45
68	A08	212	VDD	108	DQ40	252	VSS
69	A06	213	A05	109	VSS	253	DQ41
70	VDD	214	A04	110	DM5_N	254	VSS
71	A03	215	VDD	111	NC	255	DQS5_C
72	A01	216	A02	112	VSS	256	DQS5_T
73	VDD	217	VDD	113	DQ46	257	VSS
74	CK0_T	218	CK1_T	114	VSS	258	DQ47
75	CK0_C	219	CK1_C	115	DQ42	259	VSS
76	VDD	220	VDD	116	VSS	260	DQ43
77	VTT	221	VTT	117	DQ52	261	VSS
78	EVENT_N	222	PARITY	118	VSS	262	DQ53
79	A00	223	VDD	119	DQ48	263	VSS
80	VDD	224	BA1	120	VSS	264	DQ49
81	BA0	225	A10	121	DM6_N	265	VSS
82	A16	226	VDD	122	NC	266	DQS6_C
83	VDD	227	RFU	123	VSS	267	DQS6_T
84	CS0_N	228	A14	124	DQ54	268	VSS
85	VDD	229	VDD	125	VSS	269	DQ55
86	A15	230	NC	126	DQ50	270	VSS
87	ODT0	231	VDD	127	VSS	271	DQ51
88	VDD	232	A13	128	DQ60	272	VSS
89	CS1_N	233	VDD	129	VSS	273	DQ61
90	VDD	234	NC	130	DQ56	274	VSS
91	ODT1	235	NC	131	VSS	275	DQ57
92	VDD	236	VDD	132	DM7_N	276	VSS
93	NC	237	NC	133	NC	277	DQS7_C
94	VSS	238	SA2	134	VSS	278	DQS7_T
95	DQ36	239	VSS	135	DQ62	279	VSS
96	VSS	240	DQ37	136	VSS	280	DQ63
97	DQ32	241	VSS	137	DQ58	281	VSS
98	VSS	242	DQ33	138	VSS	282	DQ59
99	DM4_N	243	VSS	139	SA0	283	VSS
100	NC	244	DQS4_C	140	SA1	284	VDDSPD
101	VSS	245	DQS4_T	141	SCL	285	SDA
102	DQ38	246	VSS	142	VPP	286	VPP
103	VSS	247	DQ39	143	VPP	287	VPP
104	DQ34	248	VSS	144	NC	288	VPP

7.0 DIMM Pin Description

Pin Name	Function	Pin Name	Function
Ax	Address inputs	SDA	Serial Data
A10/AP	Auto precharge:	DQS_t,DQS_c, DQSU_t DQSU_c, DQSL_t, DQSL_c	Data strobe
A12/BC_n	Burst chop	ALERT_n	Alert output
ACT_n	Command input	EVENT_n	Temperature event
BAx	Bank address inputs	VDD	Module power Supply
BGx	Bank group address inputs	VPP	DRAM activating power supply
C0, C1, C2	Chip ID	VREFCA	Reference voltage for control, command, and address pins.
CKx_t CKx_c	Clock	VSS	Ground
CKEx	Clock enable	VTT	Power supply for termination of address, command, and control VDD/2
CSx_n	Chip select	VDDSPD	Power supply used to power the I2C bus for SPD.
ODTx	On-die termination	RFU	Reserved for future use
PARITY	Parity for command and address	NC	No connect
RAS_n/A16 CAS_n/A15 WE_n/A14	Command inputs	NF	No function
RESET_n	Active LOW asynchronous reset		
SAx	Serial address inputs		
SCL	Serial clock for temperature sensor/SPD EEPROM		
DQx, CBx	Data input/output and check bit input/output		
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n)	Input data mask and data bus inversion		



9.0 Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V
I_{VTT}	Termination reference current from V_{TT}	–750	–	750	mA
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V
IIN	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	–2.0	–	2.0	µA
IZQ	Input leakage current; ZQ	–50.0	–	10.0	µA
IOZpd	Output leakage current; V_{OUT} = V_{DD}; DQ is High-Z	–	–	10.0	µA
IOZpu	Output leakage current; V_{OUT} = V_{SS}; DQ is High-Z; ODT is disabled with ODT input HIGH	–50.0	–	–	µA
IVREFCA	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	–2.0	–	2.0	µA

9.1 SPEED EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Typ	Max	Units
Supply voltage	VDDSPD	1.7	2.5	3.6	V
Input low voltage: logic 0; All inputs	VIL	–0.5	–	VDDSPD × 0.3	V
Input high voltage: logic 1; All inputs	VIH	VDDSPD × 0.7	–	VDDSPD + 0.5	V
Output low voltage: 3mA sink current V_{DDSPD} > 2V	VOL	–	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	ILI	–	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	ILO	–	–	±5	µA

9.2 SPEED EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	tSCL	10	1000	kHz
Clock pulse width HIGH time	tHIGH	260	–	ns
Clock pulse width LOW time	tLOW	500	–	ns
Detect clock LOW timeout	tTIMEOUT	25	35	ms
SDA rise time	tR	–	120	ns
SDA fall time	tF	–	120	ns
Data-in setup time	tSU:DAT	50	–	ns
Data-in hold time	tHD:DI	0	–	ns
Data out hold time	tHD:DAT	0	350	ns
Start condition setup time	tSU:STA	260	–	ns
Start condition hold time	tHD:STA	260	–	ns
Stop condition setup time	tSU:STO	260	–	ns
Time the bus must be free before a new transition can start	tBUF	500	–	ns
Write time	tW	–	5	ms
Warm power cycle time off	tPOFF	1	–	ms
Time from power-on to first command	tINIT	10	–	ms

12.0 SPD EEPROM Operation

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module-specific parameters
2	256–319	100h–13Fh	Reserved; all bytes coded as 00h
IDD4W	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

11. Thermal Characteristics

Symbol	Parameter/Condition	Value	Units
TC	Commercial operating case temperature	0 to 85	°C
TC	Auto precharge:	>85 to 95	°C
TOPER	Normal operating	0 to 85	°C
TOPER	Extended temperature	>85 to 95	°C
TSTG	Non-operating storage temperature	–55 to 100	°C
RHSTG	Non-operating storage relative humidity (non-	5 to 95	%
NA	Change rate of storage temperature	20	°C/hour

12.0 IDD Specifications

Specifications and Conditions – 8 GB (Die Revision R)

Parameter	Symbol	IDD	Unit
One bank ACTIVATE-PRECHARGE current	IDD0	384	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I_{PP} current	IPP0	32	mA
One bank ACTIVATE-READ-PRECHARGE current	IDD1	440	mA
Precharge standby current	IDD2N	304	mA
Precharge standby ODT current	IDD2NT	328	mA
Precharge power-down current	IDD2P	240	mA
Precharge quiet standby current	IDD2Q	272	mA
Active standby current	IDD3N	344	mA
Active standby I_{PP} current	IPP3N	24	mA
Active power-down current	IDD3P	264	mA
Burst read current	IDD4R	984	mA
Burst write current	IDD4W	848	mA
Burst refresh current (1x REF)	IDD5R	376	mA
Burst refresh I_{PP} current (1x REF)	IPP5R	40	mA
Self refresh current: Normal temperature range (0°C to +85°C)	IDD6N	256	mA
Self refresh current: Extended temperature range (0°C to +95°C)	IDD6E	416	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	IDD6R	152	mA
Auto self refresh current (25°C)	IDD6A	68.8	mA
Auto self refresh current (45°C)	IDD6A	168	mA

Auto self refresh current (75°C)	IDD6A	232	mA
Auto self refresh current (95°C)	IDD6A	416	mA
Auto self refresh I_{PP} current	IPP6X	40	mA
Bank interleave read current	IDD7	1240	mA
Bank interleave read I_{PP} current	IPP7	64	mA
Maximum power-down current	IDD8	192	mA

13.0 Physical Dimensions: (1Gx8 Based, 1Gx64, 1 Rank)